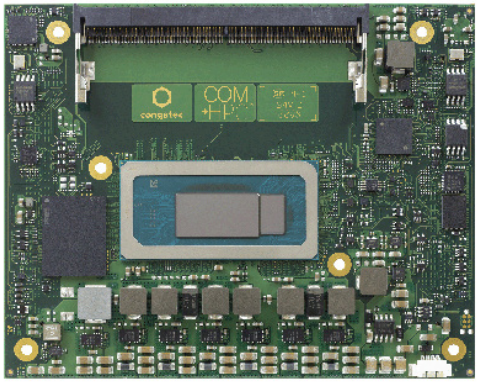

conga-HPC/cRLP

COM-HPC® 1.20 Client Size A Module with 13th Generation Intel® Processors

User's Guide

Revision 1.00

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Revision History

Revision	Date (yyyy-mm-dd)	Author	Changes
0.01	2023-07-04	BEU	• Preliminary release
1.00	2024-07-01	BEU	• Updated COM-HPC revision to 1.20 in title page, section 1.2 "The conga-HPC/cRLP" and section 9 " Signal Descriptions and Pinout Tables" • Updated title page • Added reference to additional documents to Preface section • Updated heading "Lead Free Designs (RoHS)" to "RoHS Directive" • Added COM-HPC Mini form factor to section 1.1 "COM-HPC® Concept" • Updated section 1.2 "The conga-HPC/cRLP" • Added module variant PN 044508 to Table 2 and Table 7 • Updated memory speed from 4800 to 5200 MT/s in Table 2 and Table 3 • Updated USB description in Table 4 • Updated ACPI 5.0a to ACPI 6.0 in Table 4 and section 6.19 "Power Management" • Removed MIPI CSI-2 support from Table 4, Table 20, Table 34, and section 3 "Block Diagram" • Updated supported humidity in Table 4 • Corrected PN of commercial variants in Table 7 • Added power consumption values to Table 7 • Added CMOS power consumption values to Table 8 • Added supported LTSC version to OS in section 2.2 "Supported Operating Systems" • Updated temperature and humidity values in section 2.7 "Environmental Specifications" • Added note regarding long term storage to section 2.7 "Environmental Specifications" • Updated block diagram in section 3 "Block Diagram" • Added note regarding long term storage to section 4 "Cooling Solutions" • Added caution regarding heatpipes to section 4 "Cooling Solutions" • Added note regarding MAC addresses to section 6.1 "NBASE-T Ethernet" • Added PCIe# and highlighted additional PCIe lane configuration supported by default in Table 10 • Added USB PD and retimer information to section 6.4 "USB Ports" • Updated MIPI CSI-2 support in section 6.9 "Camera Serial Interface (CSI) Ports" and Table 34 • Removed support for I2S and SoundWire from section 6.10 "Audio Interfaces", Table 17, Table 35, Table 36 • Removed support for I2C1 from Table 1, Table 17, Table 38 and section 6.12 "I2C Ports" • Added note with reference to USB PD addresses to section 6.13 "Port 80 Support on USB_PD I2C Bus" • Added note with reference to SMBus addresses to section 6.15 "SMBus" • Added section 6.18 "Inrush and Maximum Current Peaks" • Added section 7.1 "Integrated Real-Time Hypervisor" • Added reference to S5e power consumption measurements to section 7.2.4 "Enhanced Soft-Off State" • Added note to section 7.2.5 "Power Loss Control" • Added section 8.6 "Memory Population Rules" • Added note regarding USB 0 and 1 support to Table 25 and Table 26 • Corrected PU of TMDS I2C control datasignal from 100 KΩ to 2.2 KΩ in Table 32 • Corrected PU of SMBus signals from 100 KΩ to 2.2 KΩ in Table 44 • Added system resources to section 10 "System Resources"

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Preface

This user's guide provides information about the components, features, connectors and system resources available on the conga-HPC/cRLP. It is one of three documents that should be referred to when designing a COM-HPC® application. The other reference documents that should be used include the following:

COM-HPC® Module Base Specification
COM-HPC® Carrier Design Guide

These documents can be found on the PICMG® website at www.picmg.org

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Caution

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Note

Notes call attention to important information that should be observed.

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Terminology

Term	Description
cBC	congatec Board Controller
CSI	Camera Serial Interface
CSM	Compatibility Suppport Module
COM	Computer-on-Module
DDI	Digital Display Interface
DP++	DisplayPort Dual-Mode
DPoC	DisplayPort over Type-C
DTR	Dynamic Temperature Range
E-cores	Efficient-cores
eDP	Embedded DisplayPort
EUs	Execution Units
HDA	High Definition Audio
N.A	Not available
N.C	Not connected
PCH	Platform Controller Hub
PCIe	PCI Express
P-cores	Performance-cores
PEG	PCI Express Graphics
TBD	To be determined
TDP	Thermal Design Power
TPM	Trusted Platform Module
TSN	Time-Sensitive Networking

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1 Introduction

1.1 COM-HPC® Concept

COM-HPC® is an open standard defined specifically for high performance Computer-on-Modules (COMs) for embedded systems. The defined module types are client module with fixed input voltage, client module with variable input voltage and server module with fixed input voltage.

The COM-HPC® modules are available in the following form factors:

- Mini 95 mm x 70 mm
- Size A 95 mm x 120 mm
- Size B 120 mm x 120 mm
- Size C 160 mm x 120 mm
- Side D 160 mm x 160 mm
- Side E 200 mm x 160 mm

Table 1 COM-HPC® Interface Summary

Features	Classification	Mini Module Min/Max	Client Module Min/Max	Server Module Min/Max	Comment
Ethernet	NBASE-T	1 / 2	1 / 2	1 / 1	
	KR/KX	N.A	0 / 2	2 / 8	
	SGMII	0 / 2	N.A	N.A	
Storage	SATA	0 / 2	0 / 2	0 / 2	Pin is shared with PCIe on mini module
PCIe	Lane 0-47	1 / 16	4 / 48	8 / 48	Two PCIe reference clock output pairs required on mini module
	Lane 48-63	N.A	N.A	0 / 16	
	BMC	N.A	0 / 1	1 / 1	
USB	USB 2.0 Ports 0-7	6 / 8	4 / 8	4 / 8	Ports 0-5 (mini module) or ports 0-3 (server/client module) are used for USB 3.2 and USB4 if implemented.
	USB 3.2 Gen 1 or Gen 2	0 / 5	0 / 4	0 / 2	Requires one SuperSpeed Tx pair and one Rx pair per port
	USB 3.2 Gen 2x2	0 / 4	0 / 4	0 / 2	Requires two SuperSpeed Tx pairs and two Rx pairs per port
	USB4	0 / 4	0 / 4	0 / 2	USB4 ports use USB 3.2 Gen 2x2 ports
SPI	eSPI	0 / 1	0 / 1	0 / 1	
	Boot SPI	1 / 1	1 / 1	1 / 1	
	General Purpose SPI	1 / 1	1 / 1	1 / 1	

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Features	Classification	Mini Module Min/Max	Client Module Min/Max	Server Module Min/Max	Comment
BIOS Select	-	1 / 1	1 / 1	1/1	
Display	DDI	0 / 2	1 / 3	N.A	Additional display outputs may be available on the USB4 interface. On mini module, DDI pins are shared with USB4.
	eDP	0 / 1	0 / 1	N.A	
MIPI	DSI	0 / 1	0 / 1	N.A	
	CSI	N.A [1]	0 / 2	N.A	[1] Optional FFC connectors for MIPI-CSI on the mini module.
Audio	SoundWire	0 / 2	0 / 2	N.A	I2S pins may be used for one HDA port or two additional SoundWire ports for a total of up to four SoundWire ports.
	I2S	0 / 1	0 / 1	N.A	
Other Serial Ports	I2C	2 / 3	2 / 2 [2]	2 / 2	I2C0 and I2C1 for client and server modules. The mini module supports a third I2C port (I2C2/MDIO (for SGMII PHY setup). [2] The conga-HPC/cRLP does not support I2C1.
	SMBus	1 / 1	1 / 1	1 / 1	
	IPMB	N.A	0 / 1	0 / 1	
	UART	0 / 2	0 / 2	1 / 2	
GPIO	-		12 / 12	12 / 12	
Miscellaneous	Watchdog Timer	0 / 1	0 / 1	0 / 1	
	Fan (PWM and tachometer)	1 / 1	1 / 1	1 / 1	
FuSa	FuSa set of signals	0 / 1	0 / 1	0 / 1	
Power Rails	VCC	12 / 12	28 / 28	28 / 28	
	VCC_5V-SBY	N.A	0 / 2	0 / 2	The mini module does not have 5V standby pins.
	VCC_RTC	1 / 1	1 / 1	1 / 1	
	GND	All	All	All	All available GND pins shall be used.
Connector	J1	1 / 1	1 / 1	1 / 1	
	J2	N.A	0 / 1	1 / 1	

1.2 The conga-HPC/cRLP

The conga-HPC/cRLP is a COM-HPC® client module with wide range input voltage. The module uses PCB size A definition and it complies with COM-HPC® specification 1.20.

The conga-HPC/cRLP is equipped with two high performance connectors that ensure stable data throughput, and support high bandwidth networking. It provides all the core functional requirements for any embedded application when mounted onto an application-specific carrier board.

The conga-HPC/cRLP features the Intel® Core™ 13th Gen Processors Raptor Lake-P (H-Series, P-Series, U-Series) with maximum base TDP of 45 W.

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1.3 Options Information

The conga-HPC/cRLP is currently available in four commercial and four industrial variants. The tables below show the different variants:

Table 2 Commercial Variants

Part-No.		045500	045501	045502	045504	044508
Processor Number		Intel® Core™ i7-13800HE	Intel® Core™ i7-1370PE	Intel® Core™ i7-1365UE	Intel® Core™ i5-1340PE	Intel® Core™ i3-1315UE
P-Cores / E-Cores / Threads		6 / 8 / 20	6 / 8 / 20	2 / 8 / 12	4 / 8 / 16	2 / 4 / 8
P-Core Min / Base / Turbo Freq		1.80 GHz / 2.50 GHz / 5.00 GHz	1.30 GHz / 1.90 GHz / 4.80 GHz	1.20 GHz / 1.70 GHz / 4.90 GHz	1.20 GHz / 1.80 GHz / 4.50 GHz	0.80 GHz/ 1.20 GHz / 4.50 GHz
E-Core Base / Max Turbo Freq		1.80 GHz / 4.00 GHz	1.20 GHz / 3.70 GHz	1.20 GHz / 3.70 GHz	1.30 GHz / 3.30 GHz	0.90 GHz / 3.3 GHz
Cache		24 MB Intel® Smart Cache	24 MB Intel® Smart Cache	12 MB Intel® Smart Cache	12 MB Intel® Smart Cache	10 MB Intel® Smart Cache
Processor Graphics		Intel® Iris® Xe Graphics (96 EUs)	Intel® Iris® Xe Graphics (96 EUs)	Intel® Iris® Xe Graphics (96 EUs)	Intel® Iris® Xe Graphics (80 EUs)	Intel® UHD Graphics (64 EUs)
- Max Dynamic Freq		1.40 GHz	1.40 GHz	1.30 GHz	1.35 GHz	1.20 GHz
Memory Specifications		SO-DIMM DDR5 up to 5200 MT/s	SO-DIMM DDR5 up to 5200 MT/s	SO-DIMM DDR5 up to 5200 MT/s	SO-DIMM DDR5 up to 5200 MT/s	SO-DIMM DDR5 up to 5200 MT/s
- Max Memory Size		2x 32 GB (64 GB)	2x 32 GB (64 GB)	2x 32 GB (64 GB)	2x 32 GB (64 GB)	2x 32 GB (64 GB)
- # of Memory Channels		2 (Dual-Channel)	2 (Dual-Channel)	2 (Dual-Channel)	2 (Dual-Channel)	(Dual-Channel)
- ECC Memory Supported		No	No	No	No	No
Chipset		Intel® 700 Series	Intel® 700 Series	Intel® 700 Series	Intel® 700 Series	Intel® 700 Series
PCIe® Lanes	Gen 3	Up to 8 lanes	Up to 8 lanes	Up to 8 lanes	Up to 8 lanes	Up to 8 lanes
	Gen 4	8 lanes	8 lanes	8 lanes	8 lanes	8 lanes
	Gen 5	8 lanes	—	—	—	—
Ethernet Controller		Intel® i226-LM	Intel® i226-LM	Intel® i226-LM	Intel® i226-V	Intel® i226-V
- TSN Supported		Yes	Yes	Yes	No	No
CPU Use Condition [1]		Embedded Broad Market Commercial Temp	Embedded Broad Market Commercial Temp	Embedded Broad Market Commercial Temp	Embedded Broad Market Commercial Temp	Embedded Broad Market Commercial Temp
CPU Tjunction	Min.	0°C	0°C	0°C	0°C	0°C
	Max.	100°C	100°C	100°C	100°C	100°C
DTR (Cold to Hot Transition) [2]		T_{Boot} + 70°C	T_{Boot} + 70°C	T_{Boot} + 70°C	T_{Boot} + 70°C	T_{Boot} + 70°C
DTR (Hot to Cold Transition) [2]		T_{Boot} - 70°C	T_{Boot} - 70°C	T_{Boot} - 70°C	T_{Boot} - 70°C	T_{Boot} - 70°C
Processor Min / Base / Max / Turbo Power		35 W / 45 W / 65 W / 115 W	20 W / 28 W / 35 W / 64 W	12 W / 15 W / 28 W / 55 W	20 W / 28 W / 35 W / 64 W	12 W / 15 W / 28 W / 55 W

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Table 3 Industrial Variants

Part-No.		045510	045511	045512	045514
Processor Number		Intel® Core™ i7-13800HRE	Intel® Core™ i7-1370PRE	Intel® Core™ i7-1365URE	Intel® Core™ i5-1350PRE
P-Cores / E-Cores / Threads		6 / 8 / 20	6 / 8 / 20	2 / 8 / 12	4 / 8 / 16
P-Core Min / Base / Turbo Freq		1.80 GHz / 2.50 GHz / 5.00 GHz	1.30 GHz / 1.90 GHz / 4.80 GHz	1.20 GHz / 1.70 GHz / 4.90 GHz	1.20 GHz / 1.80 GHz / 4.60 GHz
E-Core Base / Turbo Freq		1.80 GHz / 4.00 GHz	1.20 GHz / 3.70 GHz	1.20 GHz / 3.70 GHz	1.30 GHz / 3.40 GHz
Cache		24 MB Intel® Smart Cache	24 MB Intel® Smart Cache	12 MB Intel® Smart Cache	12 MB Intel® Smart Cache
Processor Graphics		Intel® Iris® Xe Graphics (96 EUs)	Intel® Iris® Xe Graphics (96 EUs)	Intel® Iris® Xe Graphics (96 EUs)	Intel® Iris® Xe Graphics (80 EUs)
- Max Dynamic Freq		1.40 GHz	1.40 GHz	1.30 GHz	1.40 GHz
Memory Specifications		SO-DIMM DDR5 up to 5200 MT/s	SO-DIMM DDR5 up to 5200 MT/s	SO-DIMM DDR5 up to 5200 MT/s	SO-DIMM DDR5 up to 5200 MT/s
- Max Memory Size		2x 32 GB (64 GB)	2x 32 GB (64 GB)	2x 32 GB (64 GB)	2x 32 GB (64 GB)
- # of Memory Channels		2 (Dual-Channel)	2 (Dual-Channel)	2 (Dual-Channel)	2 (Dual-Channel)
- ECC Memory Supported		In-band ECC	In-band ECC	In-band ECC	In-band ECC
Chipset		Intel® 700 Series	Intel® 700 Series	Intel® 700 Series	Intel® 700 Series
PCIe® Lanes	Gen 3	Up to 8 lanes	Up to 8 lanes	Up to 8 lanes	Up to 8 lanes
	Gen 4	8 lanes	8 lanes	8 lanes	8 lanes
	Gen 5	8 lanes	—	—	—
Ethernet Controller		Intel® i226-IT	Intel® i226-IT	Intel® i226-IT	Intel® i226-IT
- TSN Supported		Yes	Yes	Yes	Yes
CPU Use Condition [1]		Industrial	Industrial	Industrial	Industrial
CPU Tjunction	Min.	- 40°C	- 40°C	- 40°C	- 40°C
	Max.	100°C	100°C	100°C	100°C
DTR (Cold to Hot Transition) [2]		T_{Boot} + 110°C	T_{Boot} + 110°C	T_{Boot} + 110°C	T_{Boot} + 110°C
DTR (Hot to Cold Transition) [2]		T_{Boot} - 110°C	T_{Boot} - 110°C	T_{Boot} - 110°C	T_{Boot} - 110°C
Processor Min / Base / Max / Turbo Power		35 W / 45 W / 65 W / 115 W	20 W / 28 W / 35 W / 64 W	12 W / 15 W / 28 W / 55 W	20 W / 28 W / 35 W / 64 W

Note

1. *Intel® SoC use conditions. For more information, see Intel® documentation.*

2. *T_{Boot} is the boot temperature. If the Tjunction is not within the DTR range, you must reboot the system. See Intel documentation for more information.*

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2 Specifications

2.1 Feature List

Table 4 Feature Summary

Form Factor	COM-HPC Client Size A | Client Connector Pinout
CPUs	Intel® Core™ 13th Gen Processors Raptor Lake-P (H-Series, P-Series, U-Series)
DRAM	2 SO-DIMM sockets for DDR5 memory modules up to 32 GB RAM each (max. 64 GB RAM system capacity) | up to 5200 MT/s
Mass Storage	NVMe x1 SSD (optional)
Graphics	Intel® UHD Graphics or Intel® Iris® Xe Graphics architecture | up to 96 EUs
Display	3x DDI | eDP
Ethernet	2x 2.5 GbE with TSN support via Intel® i226 Ethernet controller series
I/O Interfaces	x8 PCIe Gen5 (only available on variants based on RPL-P H series) | 2 x4 PCIe Gen4 | up to 8 PCIe Gen3 | 2x USB4 | 2x USB 3.2 Gen2x1 | up to 8x USB2.0 | up to 2x SATA | 2x UART | 12x GPIO | eSPI | SM Bus | I2C | GP-SPI
Audio	HDA
congatec Board controller	Multi Stage Watchdog | non-volatile User Data Storage | Manufacturing and Board Information | Board Statistics I²C bus (fast mode, 400 kHz, multi-master) | Power Loss Control | Hardware Health Monitoring | POST Code Redirection
Embedded BIOS Feature	AMI Aptio® UEFI firmware | 32 Mbyte serial SPI with congatec Embedded BIOS feature | OEM Logo | OEM CMOS default settings | LCD Control | Display Auto Detection | Backlight Control | Flash Update
Security	Trusted Platform Module (TPM 2.0)
Power Management	ACPI 6.0 with battery support
Operating Systems	Microsoft® Windows 11 | Microsoft® Windows 11 IoT Enterprise | Microsoft® Windows 10 | Microsoft® Windows 10 IoT Enterprise | Linux | Yocto
Hypervisor	RTS Real-Time Hypervisor
Temperature	Commercial Variants: Operation 0°C to 60°C Storage -20°C to +80°C Industrial Variants: Operation -40°C to 85°C Storage -40°C to +85°C
Humidity	Operation 10% to 85% r. H. non cond. Storage 5% to 85% r. H. non cond.
Size	120 x 95 mm

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2.2 Supported Operating Systems

The conga-HPC/cRLP supports the following operating systems:

- Microsoft® Windows 11 (64-bit)
- Microsoft® Windows 11 IoT Enterprise (64-bit)
- Microsoft® Windows 10 Enterprise 2021 LTSC (64-bit)
- Microsoft® Windows 10 IoT Enterprise 2021 LTSC (64-bit)
- Linux
- Yocto
- RTS Real-Time Hypervisor

Note

1. *The conga-HPC/cRLP supports only native UEFI Operating Systems. Legacy Operating Systems which require CSM (Compatibility Suppport Module) as part of the UEFI firmware are not supported anymore.*

2. *For Windows® 10 installation, we recommend a minimum storage capacity of 20 GB. congatec will not offer technical support for systems with less than 20 GB storage space.*

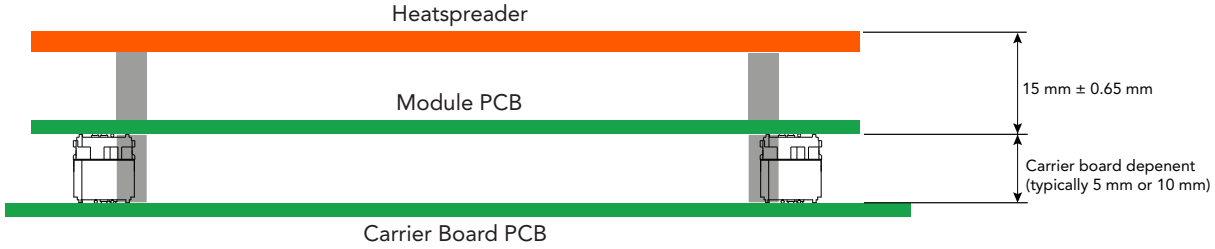
3. *To support Intel® i226 Ethernet controller in Linux by default, you need kernel 5.15 or higher.*

2.3 Mechanical Dimensions

The conga-HPC/cRLP has the following dimensions:

- length of 120 mm
- width of 95 mm
- PCB height of 2 mm +/- 10%

The overall height of an assembly is shown below:



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2.4 Supply Voltage Standard Power

The conga-HPC/cRLP requires 8 - 20 V DC input power (client module with wide range input voltage).

2.4.1 Electrical Characteristics

Power supply pins on the module's connectors limit the amount of input power. The following table provides an overview of the limitations for the conga-HPC/cRLP (client module with wide range input voltage).

Table 5 Input Power - Wide Range Vin

Power Rail	Module Pin Current Capability (Ampere)	Input Range (V)	Min. Input (V)	Max. Module Input Power at Min. Input Voltage (W)	Assumed Conversion Efficiency (%)	Max. Module Load Power at Min. Input Voltage (W)
VCC	28 * 1.12 = 31.4	8 - 20	8.0	251	85	213
VCC_5V_SBY	1.12	4.75 - 5.25	4.75	5.32	100	10.6 (with two VCC_5V_SBY pins)
VCC_RTC	1.12	2.3 - 3.3	2.3			

2.4.2 Rise Time

The input voltages shall rise from 10 percent of nominal to 90 percent of nominal within a timeframe of 0.1 ms to 20 ms. The smooth turn-on requires that, during the 10 percent to 90 percent portion of the rise time, the slope of the turn-on waveform must be positive.

2.5 Power Consumption

The power consumption values were measured with the following setup:

- conga-HPC/cRLP
- modified congatec carrier board
- conga-HPC/cRLP cooling solution
- Microsoft® Windows® 10 (64-bit)

Note

The CPU was stressed to its maximum workload with the Intel® Power and Thermal Analysis Tool.

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The power consumption values were recorded during the following system states:

Table 6 Measurement Description

System State	Description	Comment
S0: Minimum value	Lowest frequency mode (LFM) with minimum core voltage during desktop idle	
S0: Maximum value	Highest frequency mode (HFM/Turbo Boost)	The CPU was stressed to its maximum frequency
S0: Peak current	Highest current spike during the measurement of "S0: Maximum value". This state shows the peak value during runtime.	Consider this value when designing the system's power supply to ensure that sufficient power is supplied during worst case scenarios
S3	COM is powered by VCC_5V_SBY	
S5	COM is powered by VCC_5V_SBY	
S5e	COM is powered by VCC_5V_SBY	

Note

1. *The fan and SATA drives were powered externally.*

2. *All other peripherals except a DP monitor were disconnected before measurement.*

The table below provides the TDP Base power current values for the conga-HPC/cRLP at various system states:

Table 7 Power Consumption Values (TDP Base)

Part No.	Memory Size	H.W Rev.	BIOS Rev.	CPU	TDP Base	Current (Ampere) @ 12V (S0) or 5V (S3, S5, S5e)					
						S0: Min	S0: Max	S0: Peak	S3	S5	S5e
045500	2x16 GB	A.3	GRLPR003	Intel® Core™ i7-13800HE	45 W	0.59	7.36	13.81	0.35	0.27	0.0004
045501	2x16GB	A.3	GRLPR003	Intel® Core™ i7-1370PE	28 W	0.53	4.27	7.29	0.36	0.27	0.0008
045502	2x16GB	A.3	GRLPR003	Intel® Core™ i7-1365UE	15 W	0.56	2.23	6.09	0.36	0.27	0.0006
045504	2x16GB	A.3	GRLPR004	Intel® Core™ i5-1340PE	28 W	0.61	4.14	6.53	0.36	0.27	0.0006
045508	2x16GB	A.3	GRLPR004	Intel® Core™ i3-1315UE	15 W	0.47	2.49	5.67	0.42	0.24	0.0004
045510	2x16GB	A.3	GRLPR004	Intel® Core™ i7-13800HRE	45 W	0.57	7.41	13.69	0.34	0.25	0.0006
045511	2x16GB	A.3	GRLPR004	Intel® Core™ i7-1370PRE	28 W	0.56	4.31	7.32	0.35	0.25	0.0004
045512	2x16GB	A.3	GRLPR004	Intel® Core™ i7-1365URE	15 W	0.53	1.95	5.92	0.34	0.25	0.0010
045514	2x16GB	A.3	GRLPR004	Intel® Core™ i5-1350PRE	28 W	0.55	4.34	6.74	0.36	0.26	0.0006

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2.6 Supply Voltage Battery Power

The CMOS battery power consumption values for commercial and industrial module variants are listed in the table below:

Table 8 CMOS Battery Power Consumption

Module	RTC @	Voltage	Current
Commercial Variants	-10°C	3V DC	1.16 µA
	20°C	3V DC	1.40 µA
	70°C	3V DC	3.25 µA
Industrial Variants	-50°C	3V DC	1.62 µA
	20°C	3V DC	1.91 µA
	95°C	3V DC	5.68 µA

Note

1. *Do not use the CMOS battery power consumption values listed above to calculate CMOS battery lifetime.*
2. *Measure the CMOS battery power consumption of your application in worst case conditions (for example, during high temperature and high battery voltage).*
3. *Consider the self-discharge of the battery when calculating the lifetime of the CMOS battery. For more information, refer to application note AN9_RTC_Battery_Lifetime.pdf on congatec GmbH website at www.congatec.com/support/application-notes*
4. *We recommend to always have a CMOS battery present when operating the conga-HPC/cRLP.*

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2.7 Environmental Specifications

Temperature (commercial variants)	Operation: 0° to 60°C	Storage: -20° to 80°C
Temperature (industrial variants)	Operation: -40° to 85°C	Storage: -40° to 85°C
Humidity	Operation: 10% to 85%	Storage: 5% to 85%

Caution

1. *The above operating temperatures must be strictly adhered to at all times. When using a congatec heat spreader, the maximum operating temperature refers to any measurable spot on the heat spreader's surface.*
2. *Humidity specifications are for non-condensing conditions.*
3. *Disable Turbo mode for industrial use conditions.*

Note

For long term storage of the conga-HPC/cRLP (more than six months), keep the conga-HPC/cRLP in a climate-controlled building at a constant temperature between 5°C and 40°C, with humidity of less than 65% and at an altitude of less than 3000 m. Also ensure the storage location is dry and well ventilated.

We do not recommend storing the conga-HPC/cRLP for more than five years under these conditions.

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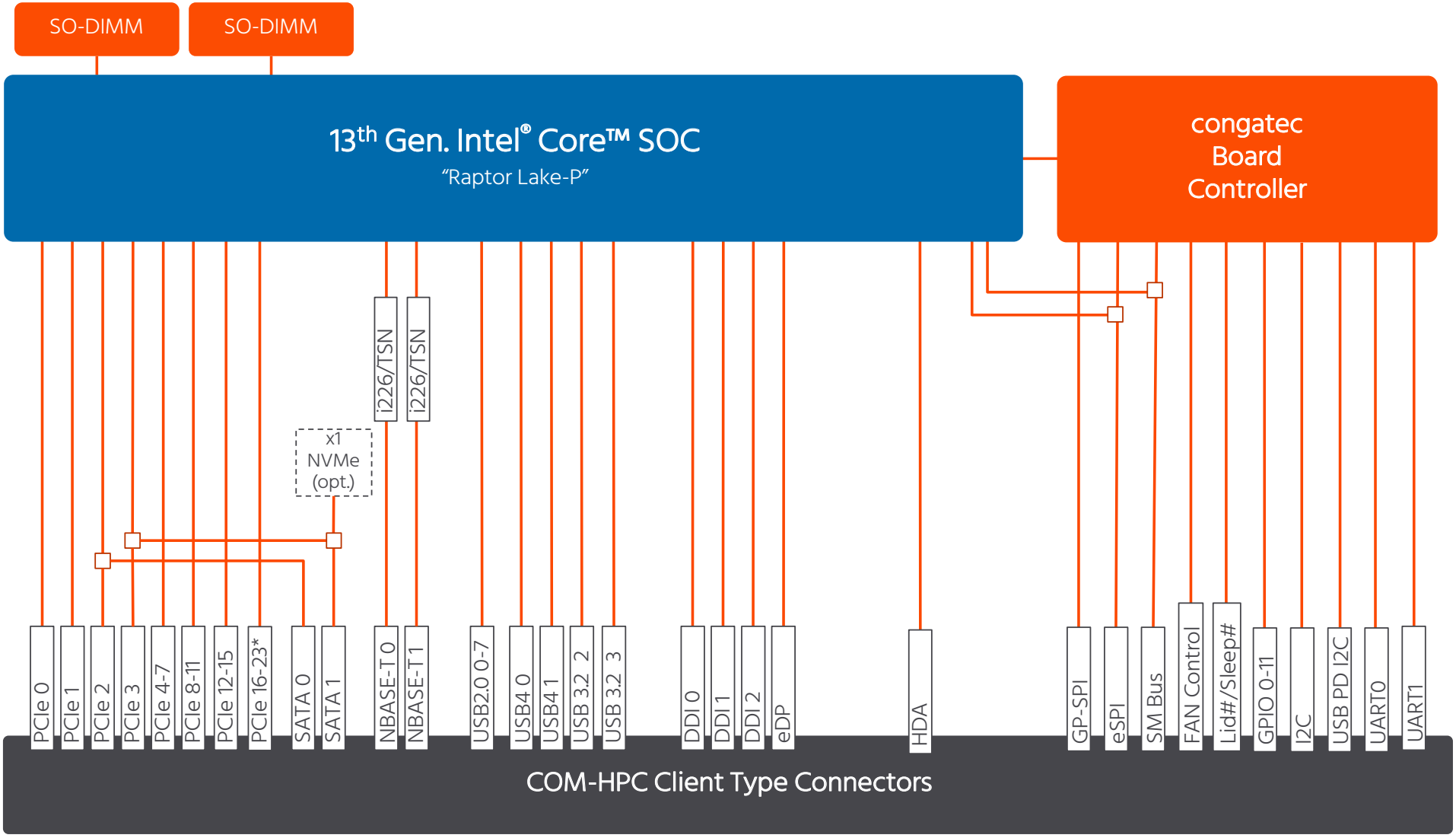
3 Block Diagram



** available only on variants based on RPL-P H-Series*

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4 Cooling Solutions

congatec GmbH offers the following cooling solutions for the conga-HPC/cRLP. The dimensions of the cooling solutions are shown in the sub-sections. All measurements are in millimeters.

Table 9 Cooling Solution Variants

Cooling Solution	Part No	Description
CSA	049550	Active cooling solution with 2.7 mm bore-hole standoffs
	049551	Active cooling solution with M2.5 threaded standoffs
CSP	049552	Passive cooling solution with 2.7 mm bore-hole standoffs
	049553	Passive cooling solution with M2.5 threaded standoffs
HSP	049554	Heatspreader with 2.7 mm bore-hole standoffs
	049555	Heatspreader with M2.5 threaded standoffs

Caution

1. *The congatec heatspreaders/cooling solutions are tested only within the commercial temperature range of 0° to 60°C. Therefore, if your application that features a congatec heat spreader/cooling solution operates outside this temperature range, ensure the correct operating temperature of the module is maintained at all times. This may require additional cooling components for your final application's thermal solution.*

2. *The heatpipes of congatec heatspreaders/cooling solutions are filled with water by default. To ensure optimal cooling performance, they should not be stored at temperatures below -20°C. If the storage temperature drops below -10°C, the heatpipes should be pre-heated before operation. Optionally, the heatpipes can be filled with acetone instead. For more information, contact your local sales representative.*

3. *For adequate heat dissipation, use the mounting holes on the cooling solution to attach it to the module. Apply thread-locking fluid on the screws if the cooling solution is used in a high shock and/or vibration environment. To prevent the standoff from stripping or cross-threading, use non-threaded carrier board standoffs to mount threaded cooling solutions.*

4. *For applications that require a vertically-mounted cooling solution, use only coolers that secure the thermal stacks with fixing post. Without the fixing post feature, the thermal stacks may move.*

5. *Do not exceed the recommended maximum torque. Doing so may damage the module or the carrier board, or both.*

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Note

1. *We recommend a maximum torque of 0.4 Nm for carrier board mounting screws and 0.5 Nm for module mounting screws.*
2. *The gap pad material used on congatec heat spreaders may contain silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.*
3. *For optimal thermal dissipation, do not store the congatec cooling solutions for more than six months.*

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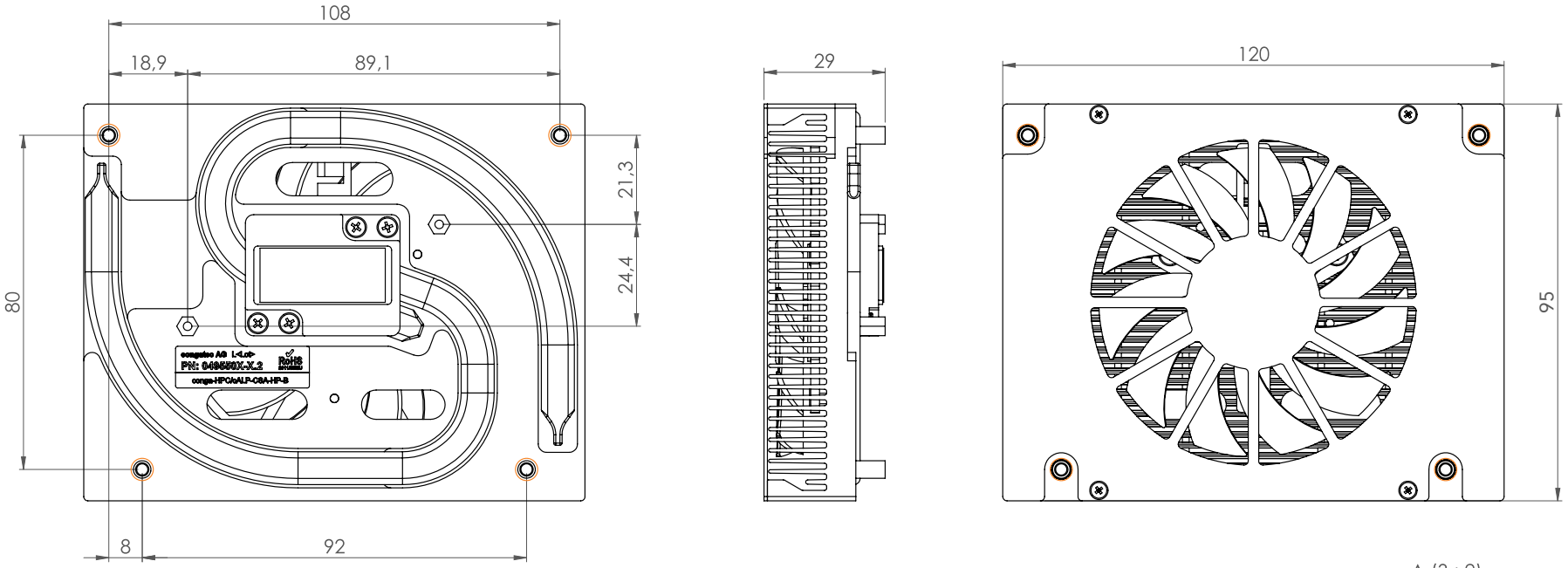
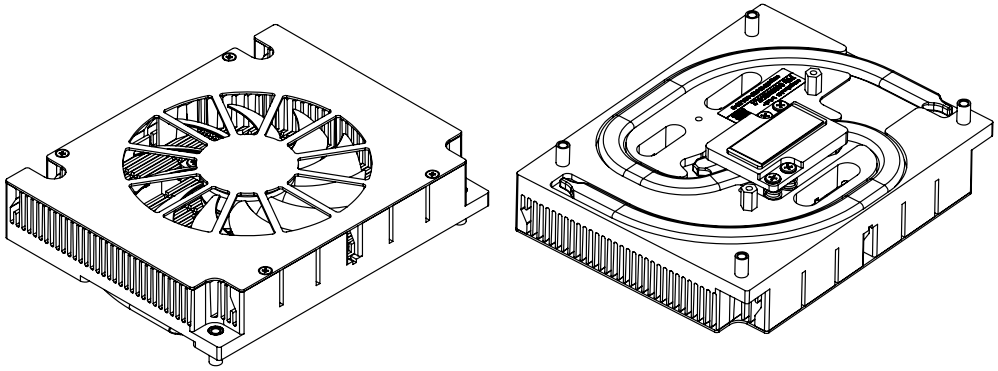
4.1 CSA Dimensions





M2.5 x 11 mm threaded standoff for threaded version
or
ø2.7 x 11 mm non-threaded standoff for borehole version

FIRST ANGLE
projection

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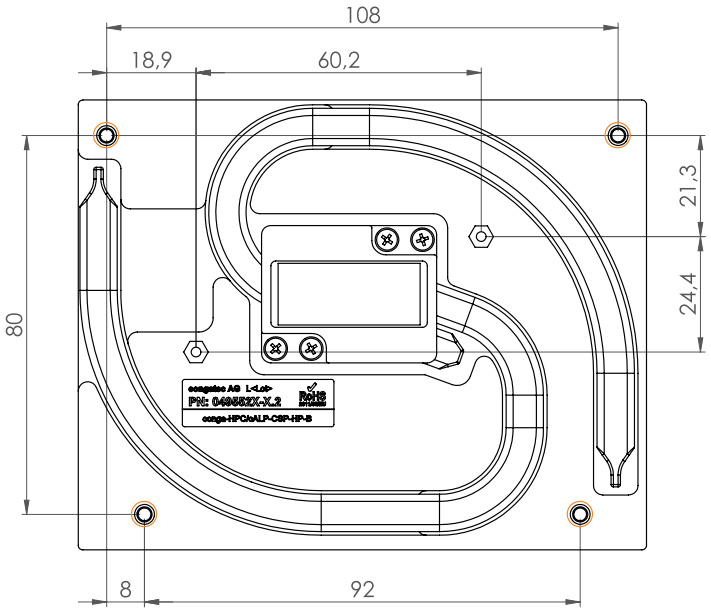
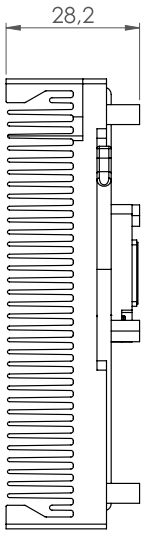
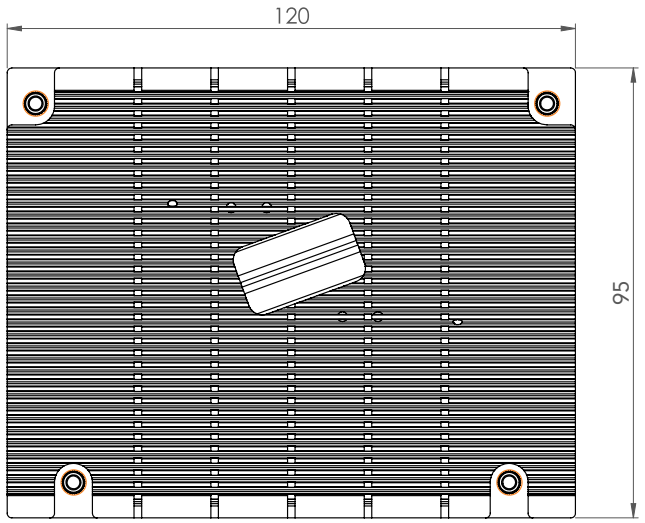
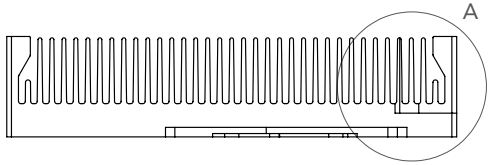
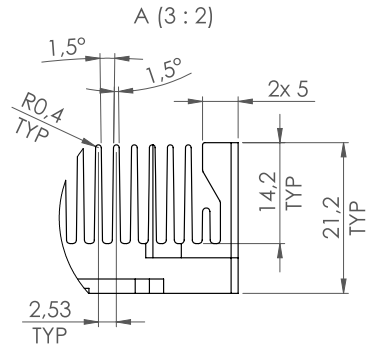
4.2 HSP Dimensions

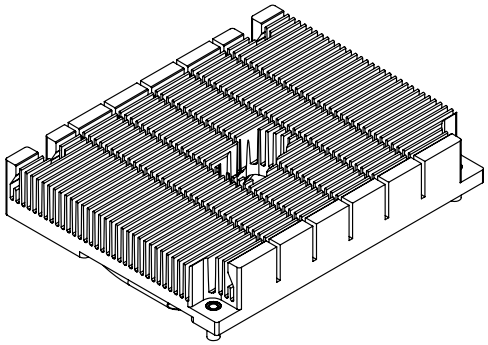


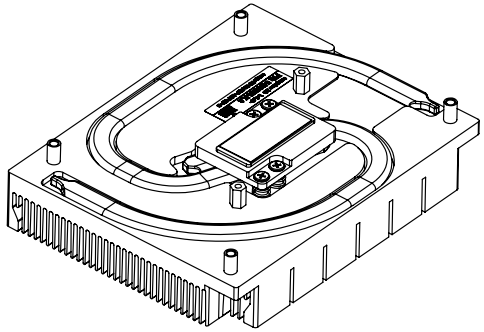








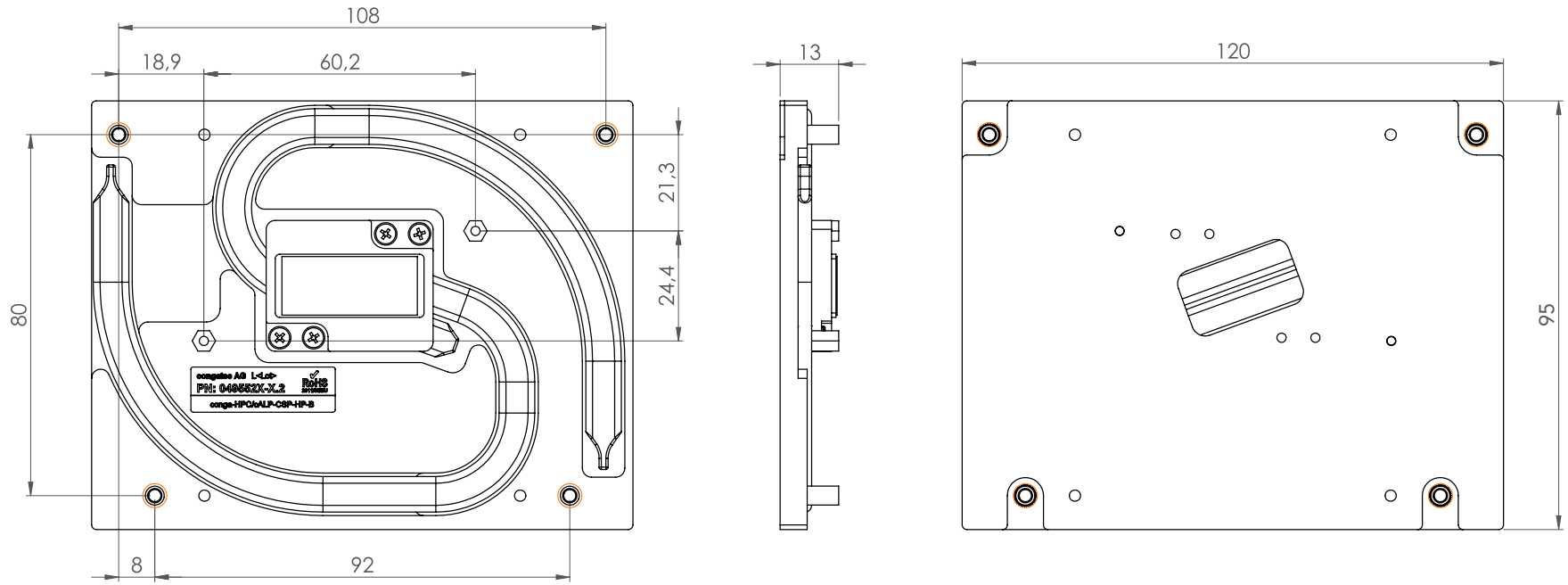


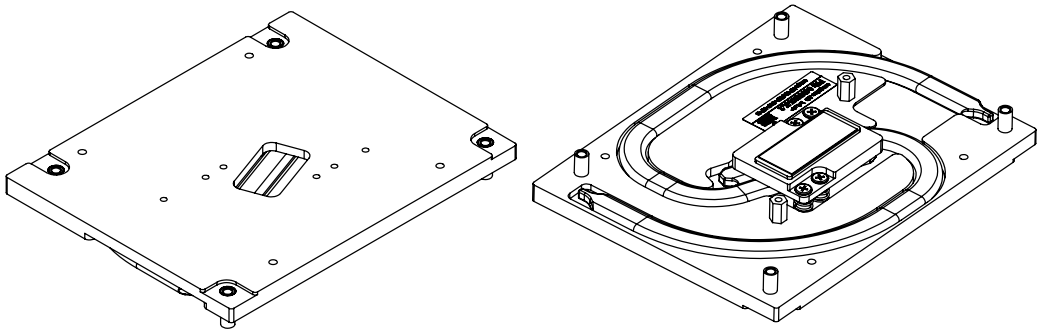


M2.5 x 11 mm threaded standoff for threaded version
or
ø2.7 x 11 mm non-threaded standoff for borehole version

FIRST ANGLE projection

4.3 HSP Dimensions





M2.5 x 11 mm threaded standoff for threaded version
or
ø2.7 x 11 mm non-threaded standoff for borehole version

FIRST ANGLE projection

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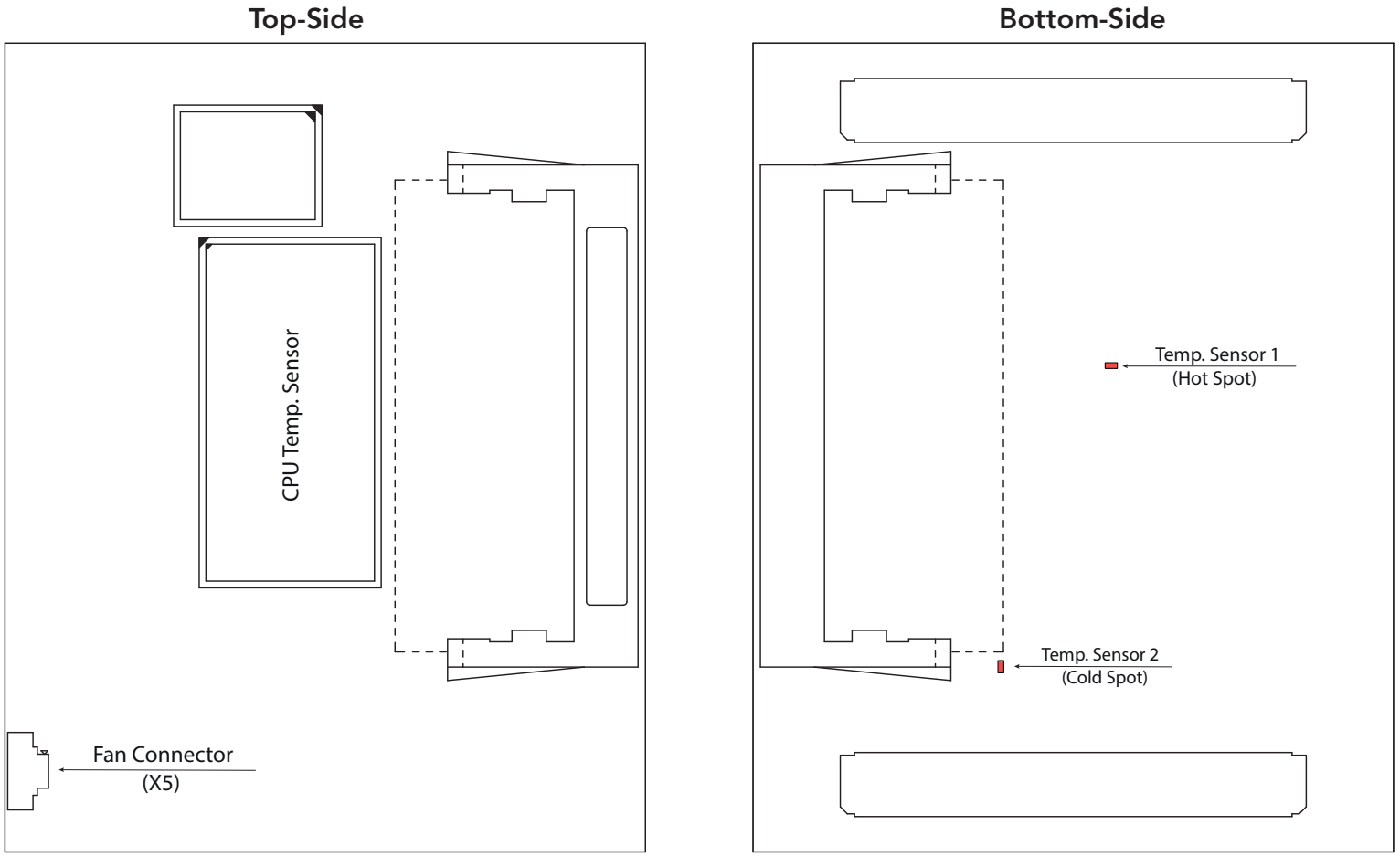
5 Onboard Temperature Sensors

The conga-HPC/cRLP features one temperature sensor on the top-side and two temperature sensors on the bottom-side. The location of each sensor and the fan connector (X5) is indicated in the drawings below:



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6 Connector Rows

The conga-HPC/cRLP is connected to the carrier board via two 400-pin connectors (COM-HPC® Client Module pinout). These connectors are broken down into eight rows. The primary connector J1 consists of rows A, B, C, and D. The secondary connector J2 consists of rows E, F, G, and H. The following subsystems can be found on these connector rows.

6.1 NBASE-T Ethernet

The conga-HPC/cRLP offers two 2.5 Gigabit Ethernet interfaces (ETH[0:1]) via two onboard Intel® i226-LM/IT/V controllers. The interfaces support:

- full-duplex operation at 10/100/1000/2500 Mbps
- half-duplex operation at 10/100 Mbps
- Intel® Active Management Technology (AMT) for industrial variants (Intel® i226-LM/IT controllers)
- Time-Sensitive Networking (TSN) [1]

Note

1. *Not supported in Windows® Operating Systems and by Intel® i226-V controller (see section 1.3 "Options Information").*
2. *The MAC address of the Intel i226 Ethernet controller is preprogrammed by default. The MAC address cannot be reprogrammed. If you require custom MAC address, contact your local sales representative.*

6.2 Serial ATA

The conga-HPC/cRLP offers two Serial ATA interfaces (SATA[0:1]) by default. The interfaces support:

- independent DMA operation
- SATA specification 3.2
- data transfer rates up to 6.0 Gb/s
- AHCI mode using memory space and RAID mode
- Hot-plug detect

Optionally, the PCIE[02:03] lanes can be enabled instead of SATA[0:1] (BIOS Setup option). SATA1 and PCIE03 cannot be enabled if the optional onboard NVMe SSD is assembled.

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Note

The SATA interfaces do not support IDE legacy mode using I/O space.

6.3 PCI Express (PCIe)

The conga-HPC/cRLP can support the PCIe® link configurations listed in the table below:

Table 10 Supported PCIe® Link Configurations

Lane	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23
Link	x1	x1	x1	x1	x1	x1	x1	x1	x1	–			x1	–			x1	–						
	x2		x2		x2		x2		x2	–			x2	–			x2	–						
	x4				x4				x4				x4				x4				–			
	–								–								x8							
Gen	3								4								5							
Source	PCH								CPU								CPU							
HSIO#	08	09	10	11	04	05	06	07	–								–							
PCIe#	09	10	11	12	05	06	07	08	(PCIE4 B)				(PCIE4 A)				(PCIE8)							

Note

1. *Lanes 00:07 collectively support a maximum of 4 links. This is a limitation of the PCH.*
2. *Lanes 02:03 are disabled by default. The lanes can be enabled in BIOS Setup instead of SATA0 and SATA1 respectively.*
3. *If the optional onboard NVMe SSD is assembled, lane 03 and SATA1 are disabled and the remaining PCH lanes support max. 3 links.*
4. *Lanes 16:23 are offered by H-Series CPUs only (e.g., Intel® Core™ i7-13800HE and i7-13800HRE).*
5. *Default link width. Optional link configurations require a customized BIOS.*

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6.4 USB Ports

The conga-HPC/cRLP can support the USB ports listed in the table below:

Table 11 Supported USB Ports

USB Port	0	1	2	3	4	5	6	7
USB 1.0	x	x	x	x	x	x	x	x
USB 1.1	x	x	x	x	x	x	x	x
USB 2.0	x	x	x	x	x	x	x	x
USB 3.2 Gen 1x1	x	x	x	x				
USB 3.2 Gen 2x1	x	x	x	x				
USB 3.2 Gen 2x2	x	x						
USB4 Gen 2x2	x	x						
USB4 Gen 3x2	x	x						
DisplayPort over Type-C (DPoC)	x	x						

Note

USB ports 0 and 1 require a PD controller and retimer to function with the default BIOS. Optionally, these ports may be used as USB 2.0 ports (or lower) without a PD controller and retimer (Custom BIOS Option).

USB PD controllers and retimers implemented on the carrier board must use the SMLink addresses listed in the table below:

Table 12 USB PD Controller and Retimer Addresses

USB Port	0	1	2	3
USB PD Controller:				
- SML1 Address	0x21	0x25	0x20	0x24
Thunderbolt Retimer:				
- SML0 Address (7-bit)	55	56	57	58

Note

The conga-HPC/cRLP has been tested and confirmed to work with the TI TPS65994AE USB PD Controller and Intel® JHL8040R Thunderbolt® Retimer.

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6.5 eSPI Interface

The conga-HPC/cRLP offers an eSPI interface for general purpose carrier board devices such as Super I/O, FPGAs, CPLDs and so on. The interface offers one chip select pin (eSPI_CS0#) for carrier board devices. eSPI_CS1# is not supported.

Unlike an LPC interface, the eSPI interface runs from a 1.8 V supply.

6.6 Boot SPI Interface

The conga-HPC/cRLP offers a Boot SPI interface for a carrier-based SPI BIOS flash device. The congatec onboard flash device (Winbond W25R256JV) and TPM device (Infineon SLB9672) are also connected to this Boot SPI interface.

The pins to select the carrier-based SPI BIOS flash device are described in the section 6.7 "BIOS Boot Selection" below.

Note

1. *The power supply to the carrier board SPI (VCC_BOOT_SPI) is 3.3 V.*

2. *The onboard SPI flash is disabled when the carrier board SPI flash is enabled.*

6.7 BIOS Boot Selection

The boot select pins BSEL0-BSEL2 are configured to load the BIOS firmware from the conga-HPC/cRLP by default. Optionally, you can configure these pins to load the BIOS firmware from the carrier board SPI flash as described in the table below:

Table 13 BIOS Select Options

BSEL2	BSEL1	BSEL0	Boot Option
1	1	1	Boot from module SPI flash (default)
1	1	0	Boot from carrier board SPI flash

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6.8 Display Interfaces

The conga-HPC/cRLP offers four dedicated display interfaces:

- three DP++ interfaces up to HBR3 (8.1 Gbps lane rate)
- one eDP™ interface up to HBR3 (8.1 Gbps lane rate)

The table below shows the supported display combinations and resolutions:

Table 14 Display Combinations and Resolutions

DDI0		DDI1		DDI2		eDP	
Interface	Max. Resolution	Interface	Max. Resolution	Interface	Max. Resolution	Interface	Max. Resolution
DP++	4096x2304 @ 60 Hz, 36 bpp	DP++	4096x2304 @ 60 Hz, 36 bpp	DP++	4096x2304 @ 60 Hz, 36 bpp	eDP	4096x2304 @ 60 Hz, 36 bpp

Note

A single DP display supports max. 7680 x 4320 @ 60Hz, 30 bpp with DSC. A single eDP™ display supports max. 5120 x 3200 @ 120Hz, 30 bpp with DSC. The actual display resolution dependents on several design factors and therefore may be lower on your system.

6.8.1 DisplayPort Dual-Mode (DP++)

The conga-HPC/cRLP offers three DP++ interfaces (DDI[0:2]). Each interface supports:

- VESA® DisplayPort™ Standard 1.4a
- HDCP 2.3 and 1.4 content protection
- Various audio formats

6.8.2 Embedded DisplayPort (eDP)

The conga-HPC/cRLP offers one eDP™ interface. This interface supports:

- VESA® Embedded DisplayPort™ Standard 1.4b
- Spread-Spectrum Clocking
- eDP™ display authentication

Note

The eDP™ interface does not support HDCP.

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6.9 Camera Serial Interface (CSI) Ports

The conga-HPC/cRLP offers two MIPI CSI-2® compatible input ports (CSI[0:1]) with support for x2 and x4 lane configurations.

Note

MIPI CSI-2® requires driver support from the silicon vendor. The driver was not available at the time of writing. Contact congatec support for more information.

6.10 Audio Interfaces

The conga-HPC/cRLP offers one Intel® High Definition Audio (HDA) interface.

6.11 Asynchronous Serial Port Interfaces

The conga-HPC/cRLP offers two 16C550 compatible UART interfaces (UART[0:1]) via the congatec Board Controller by default. The interfaces support hardware handshake, flow control, and up to 115200 baud rate.

6.12 I²C Ports

The conga-HPC/cRLP offers one I²C port (I2C0) via the congatec Board Controller with support for multi-master and fast mode.

Note

1. *I2C1 is not supported.*
2. *For the reserved I²C bus addresses, refer to section 10.3 "I2C".*
3. *You need the congatec CGOS driver and API to access the I²C interface.*

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6.13 Port 80 Support on USB_PD I2C Bus

The conga-HPC/cRLP offers BIOS Port 80h debug information over the USB Power Delivery I²C Bus (USB_PD_I2C_DAT and USB_PD_I2C_CLK). The debug information is serialized and must be deserialized on the carrer board. For information on how to deserialize and display the debug information on carrier board 7-segment displays, refer to the COM-HPC® Carrier Design Guide.

Note

For the USB_PD I2C addresses, refer to section 10.5 "USB PD Bus".

6.14 General Purpose SPI Port

The conga-HPC/cRLP offers a general purpose SPI port and two chip selects (GPSPI_CS[0:1]) via the congatec Board Controller by default.

Optionally, the general purpose SPI port can be provided via the Intel® chipset instead (assembly option).

6.15 SMBus

The conga-HPC/cRLP offers a System Management Bus (SMBus) via the Intel® chipset. The SMBus can be either always connected or isolated via a switch (BIOS Setup option).

Note

Make sure the address space of the carrier board SMBus devices does not overlap with the address space of the module devices. For the reserved SMBus addresses, refer to section 10.4 "SMBus".

6.16 General Purpose Input Outputs (GPIOs)

The conga-HPC/cRLP offers 12 general purpose inputs and outputs (GPIO_[00:11]) via the congatec Board Controller.

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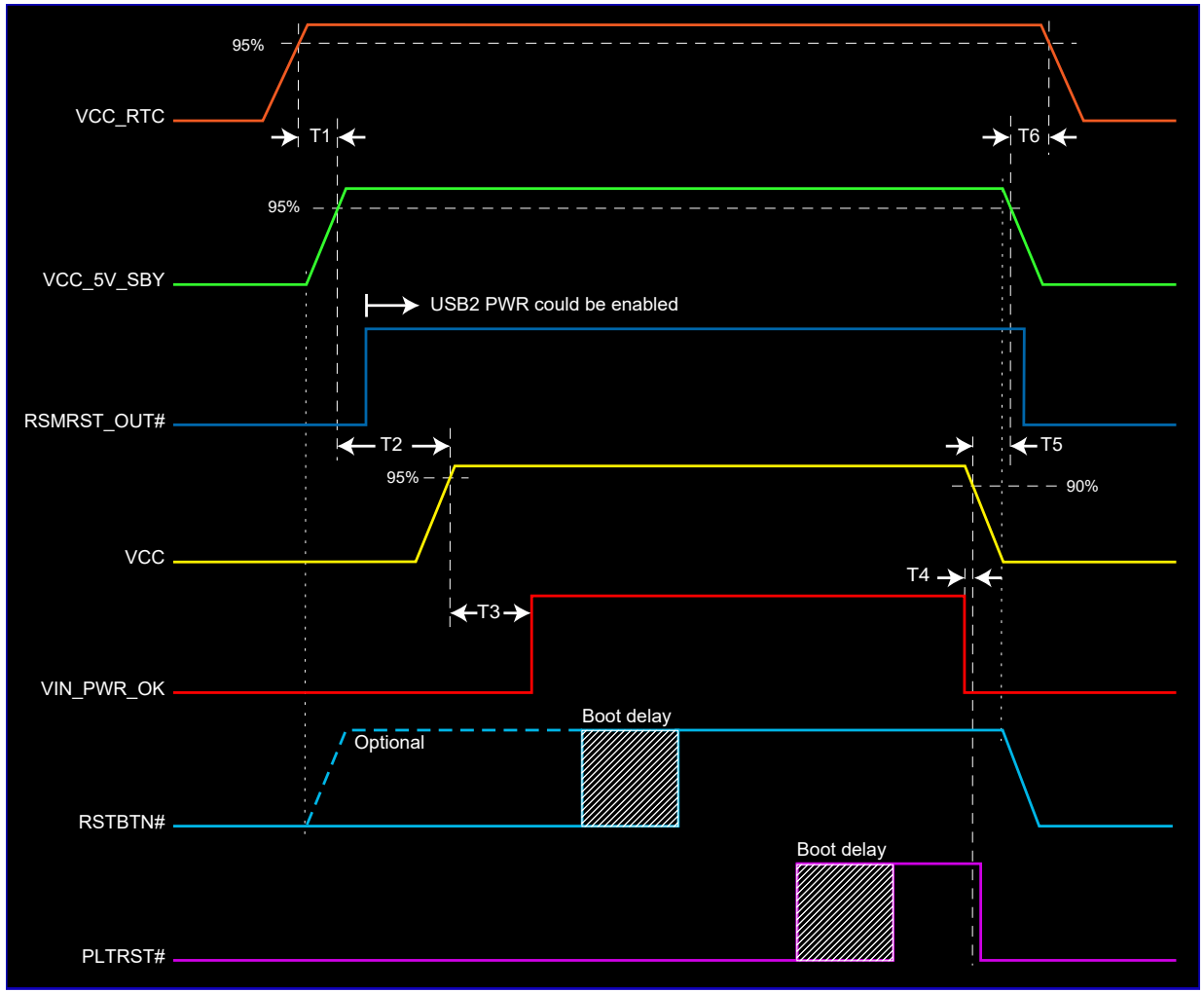
6.17 Power Control

The conga-HPC/cRLP operates over a range of 8 V to 20 V input power. Its power-up sequence is illustrated below:



The power control signals VIN_PWR_OK, RSTBTN#, SUS_S3#, and PWRBTN# are described below. For more information, refer to the COM-HPC® Module Base Specification.

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VIN_PWR_OK

Power OK from main power supply or carrier board voltage regulator circuitry. A high value indicates that the power is good and the module can start its onboard power sequencing. Carrier board hardware should not drive VIN_PWR_OK low after the input power is stable. Hold RSTBTN# low instead to keep the module in a reset condition if necessary.

SUS_S3#

The SUS_S3# signal is an active-low output that can be used to turn on the main outputs of an ATX-style power supply. To accomplish this, invert the signal on the carrier board with an inverter or transistor that is supplied by standby voltage. With SUS_S3#, the conga-HPC/cRLP can control ATX-style power supplies.

Note

If you do not use an ATX power supply, the conga-HPC/cRLP VCC_5V_SBY pins should be left unconnected.

PWRBTN#

When using ATX-style power supplies, PWRBTN# is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

6.18 Inrush Current

The table below compares the inrush current and slew rate values of the conga-HPC/cRLP at different voltage ramp durations.

Table 15 Inrush Current

Power Rail	Inrush Current [A]	Slew Rate [kV/s]	Voltage Ramp [ms]	Comment
VCC	46.40	24.41	0.394	Worst-case scenario
VCC_5V_SBY	8.40	35.11	0.115	
VCC	11.20	9.43	1.020	Typical scenario
VCC_5V_SBY	1.16	3.83	1.055	

Note

Ensure the power supply and decoupling capacitors on the carrier board are adequate for proper power sequencing.

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6.19 Power Management

ACPI

The conga-HPC/cRLP supports Advanced Configuration and Power Interface (ACPI) specification, revision 6.0. It also supports Suspend to RAM (S3). For more information, see section 8.5 "ACPI Suspend Modes and Resume Events".

DEEP Sx

The Deep Sx is a lower power state employed to minimize the power consumption while in S3/S4/S5. In the Deep Sx state, the system entry condition determines if the system context is maintained or not. All power is shut off except for minimal logic which supports limited set of wake events for Deep Sx. The Deep Sx on resumption, puts system back into the state it is entered from. In other words, if Deep Sx state was entered from S3 state, then the resume path will place system back into S3.

S5e Power State

The conga-HPC/cRLP features a congatec proprietary Enhanced Soft-Off power state, described in section 7.2.4 "Enhanced Soft-Off State".

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7 Additional Features

The following additional features are available on the conga-HPC/cRLP.

7.1 Integrated Real-Time Hypervisor

The RTS Hypervisor is integrated into the congatec firmware on the conga-HPC/cRLP by default. The integrated RTS Hypervisor offers a 30-day free evaluation license. The 30-day evaluation starts when the customer receives the x86-based modules. To access the full package, contact congatec Sales team via the online "Request Quote" button for your particular product at https://www.congatec.com/en/products/hypervisor-products/.

To activate the RTS Hypervisor, change the “Boot Device” in the BIOS setup menu to “Integrated RTS Hypervisor”.

1. Press F2 or DEL during POST to enter the BIOS setup menu.
2. Go to the Boot tab to enter the Boot setup screen.
3. Select “Integrated RTS Hypervisor" as “1st Boot Device”.
4. Go to the Save & Exit tab and select “Save Changes and Exit”.

For more information about the integrated Hypervisor, see the congatec Application Note AN56_Hypervisor_on_Module.pdf on the congatec website at https://www.congatec.com/en/support/application-notes/.

Note

1. *The configuration steps and the BIOS setup menu above are valid for "Type Based Boot Priority". For "UEFI Boot Priority", the BIOS setup menu may differ.*
2. *The Real-Time Operating System images, driver packages for the General-Purpose Operating System and the installation procedures for the Operating Systems are available for download under the "Technical information" section, in the restricted area of congatec website at www.congatec.com/login. If you require login access, contact your local sales representative.*

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7.2 congatec Board Controller (cBC)

The conga-HPC/cRLP is equipped with a Microchip microcontroller. This onboard microcontroller plays an important role for most of the congatec embedded/industrial PC features. It fully isolates some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in a low power mode. It also ensures that the congatec embedded feature set is fully compatible amongst all congatec modules.

The congatec Board Controller (cBC) supports the following features:

- Board information (See section 7.2.1)
- Watchdog (See section 7.2.2)
- Asynchronous Serial Port Interfaces (See section 6.11)
- I²C Ports (See section 6.12)
- Port 80 Support on USB_PD I2C Bus (See section 6.13)
- General Purpose SPI Port (See section 6.14)
- SMBus (See section 6.15)
- General Purpose Input Outputs (GPIOs) (See section 6.16)
- Fan Control (See section 7.2.3)
- Enhanced Soft-Off State (See section 7.2.4)
- Power Loss Control (See section 7.2.5)

7.2.1 Board Information

The cBC provides a rich data-set of manufacturing and board information such as serial number, EAN number, hardware and firmware revisions, and so on. It also keeps track of dynamically changing data like runtime meter and boot counter.

7.2.2 Watchdog

The cBC provides a multi stage watchdog solution that is triggered by software. For more information about the Watchdog feature, refer to the application note AN3_Watchdog.pdf available at www.congatec.com.

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7.2.3 Fan Control

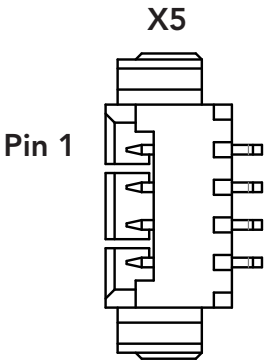
The cBC provides signals for a primary and secondary fan. Signals for the primary fan are routed to onboard connector X5. Signals for the secondary fan are routed to the COM-HPC® connector.

For the location of the onboard connector and information about the temperature sensors, see section 5 "Onboard Temperature Sensors".

The pinout of the primary fan connector (X5) is described in the table below:

Table 16 Primary Fan Connector (X5) Pinout

Pin	Signal
1	GND
2	+12V_FAN (max. 700mA)
3	CPU_FAN_TACHIN
4	CPU_FAN_PWMOUT



Connector Type

X5: 4x1 pins, 1.25mm pitch (Molex 53261-0471); Possible Mating Connector: Molex 51021-0400

Note

A four wire fan must be used to generate the correct speed readout.

7.2.4 Enhanced Soft-Off State

The cBC provides an enhanced Soft-Off state (S5e)—a congatec proprietary low-power Soft-Off state. In this state, the CPU module switches off almost all the onboard logic to reduce the power consumption (see section 2.5 "Power Consumption").

The S5e supports power button, sleep button and SMBALERT# wake events. Refer to congatec application note AN36_S5e_Implementation.pdf for detailed description of the S5e state.

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7.2.5 Power Loss Control

The cBC provides the power loss control feature. The power loss control feature determines the behaviour of the system after an AC power loss occurs. This feature applies to systems with ATX-style power supplies which support standby power rail.

The term "power loss" implies that all power sources, including the standby power are lost (G3 state). Once power loss (transition to G3) or shutdown (transition to S5) occurs, the board controller continuously monitors the standby power rail. If the standby voltage remains stable for 30 seconds, the cBC assumes the system was switched off properly. If the standby voltage is no longer detected within 30 seconds, the module considers this an AC power loss condition.

The power loss control feature has three different modes that define how the system responds when standby power is restored after a power loss occurs. The modes are:

- Turn On: The system is turned on after a power loss condition
- Remain Off: The system is kept off after a power loss condition
- Last State: The board controller restores the last state of the system before the power loss condition

Note

1. *If a power loss condition occurs within 30 seconds after a regular shutdown, the cBC may incorrectly set the last state to "ON".*
2. *The settings for power loss control have no effect on systems with AT-style power supplies which do not support standby power rail.*
3. *The 30 seconds monitoring cycle applies only to the "Last State" power loss control mode.*

7.3 OEM BIOS Customization

The conga-HPC/cRLP is equipped with congatec Embedded BIOS, which is based on American Megatrends Inc. Aptio UEFI firmware. The congatec Embedded BIOS allows system designers to modify the BIOS. For more information about customizing the congatec Embedded BIOS, refer to the congatec System Utility user's guide CGUTLm1x.pdf on the congatec website at www.congatec.com or contact technical support.

The supported customization features are described in the following sub-sections.

7.3.1 OEM Default Settings

This feature allows system designers to create and store their own BIOS default configuration. Customized BIOS development by congatec for OEM default settings is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. For information on how to add OEM default settings to the congatec Embedded BIOS, refer to the application note AN8_Create_OEM_Default_Map.pdf available at www.congatec.com.

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7.3.2 OEM Boot Logo

This feature allows system designers to replace the standard text output displayed during POST with their own BIOS boot logo. Customized BIOS development by congatec for OEM Boot Logo is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. For information on how to add an OEM boot logo to the congatec Embedded BIOS, refer to the application note AN11_Create_And_Add_Bootlogo.pdf available at www.congatec.com.

7.3.3 OEM POST Logo

This feature allows system designers to replace the congatec POST logo displayed in the upper left corner of the screen during BIOS POST with their own BIOS POST logo. Use the congatec system utility CGUTIL 1.5.4 or later to replace/add the OEM POST logo.

7.3.4 OEM DXE Driver

This feature allows designers to add their own UEFI DXE driver to the congatec embedded BIOS. Contact congatec technical support for more information on how to add an OEM DXE driver.

7.4 congatec Battery Management Interface

To facilitate the development of battery powered mobile systems based on embedded modules, congatec GmbH defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (for example, charge state of the battery, information about the battery, alarms/events for certain battery states and so on) without the need for additional modifications to the system BIOS.

In addtion to the ACPI-Compliant Control Method Battery mentioned above, the latest versions of the conga-HPC/cRLP BIOS and board controller firmware also support LTC1760 battery manager from Linear Technology and a battery only solution (no charger). All three battery solutions are supported on the I^2C bus and the SMBus. This gives the system designer more flexibility when choosing the appropriate battery sub-system. For more information about the supported Battery Management Interface, contact your local sales representative.

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7.5 API Support (CGOS)

In order to benefit from the above mentioned non-industry standard feature set, congatec provides an API that allows application software developers to easily integrate all these features into their code. The CGOS API (congatec Operating System Application Programming Interface) is the congatec proprietary API that is available for all commonly used Operating Systems such as Win32, Win64, Win CE, Linux. The architecture of the CGOS API driver provides the ability to write application software that runs unmodified on all congatec CPU modules. All the hardware related code is contained within the congatec embedded BIOS on the module. See section 1.1 of the CGOS API software developers guide, available at www.congatec.com.

7.6 Security Features

The conga-HPC/cRLP is equipped with an onboard SPI TPM 2.0 (Infineon SLB 9672VU2.0 FW15 for commercial variants or SLB 9672XU2.0 FW15 for industrial variants).

7.7 Suspend to Ram

The conga-HPC/cRLP supports the power saving mode Suspend to RAM (S3).

7.8 PCIe NVMe SSD (Optional)

Optionally, the conga-HPC/cRLP can offer an onboard PCIe NVMe SSD (Micron 2100AI; assembly option).

The NVMe SSD is currently available with the following storage capacities:

- 64 GB
- 128 GB
- 256 GB
- 512 GB
- 1 TB

Note

The conga-HPC/cRLP can either support the optional onboard PCIe NVMe SSD, PCIe03, or SATA1.

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8 conga Tech Notes

The conga-HPC/cRLP has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features.

8.1 Adaptive Thermal Monitor and Catastrophic Thermal Protection

Intel® Xeon, Core™ i9/i7/i5/i3 and Celeron® processors have a thermal monitor feature that helps to control the processor temperature. The integrated TCC (Thermal Control Circuit) activates if the processor silicon reaches its maximum operating temperature. The activation temperature that the Intel® Thermal Monitor uses to activate the TCC can be slightly modified via TCC Activation Offset in BIOS setup submenu "CPU submenu".

The Adaptive Thermal Monitor controls the processor temperature using two methods:

- Adjusting the processor's operating frequency and core voltage (EIST transitions)
- Modulating (start/stop) the processor's internal clocks at a duty cycle of 25% on and 75% off

When activated, the TCC causes both processor core and graphics core to reduce frequency and voltage adaptively. The Adaptive Thermal Monitor will remain active as long as the package temperature remains at its specified limit. Therefore, the Adaptive Thermal Monitor will continue to reduce the package frequency and voltage until the TCC is de-activated. Clock modulation is activated if frequency and voltage adjustments are insufficient. Additional hardware, software driver, or operating system support is not required.

Intel® Core™ i7/i5/i3, Celeron® and Pentium® processors use the THERMTRIP# signal to shut down the system if the processor's silicon reaches a temperature of approximately 125°C. The THERMTRIP# signal activation is completely independent from processor activity and therefore does not produce any bus cycles.

Note

1. *For THERMTRIP# to switch off the system automatically, use an ATX style power supply.*

2. *The maximum operating temperature for Intel® Xeon, Core™ i9/i7/i5/i3, and Celeron® processors is 100°C.*

3. *To ensure that the TCC is active for only short periods of time, thus reducing the impact on processor performance to a minimum, it is necessary to have a properly designed thermal solution. The Intel® Xeon, Core™ i9/i7/i5/i3, and Celeron® processor's respective datasheet can provide you with more information about this subject.*

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8.2 Processor Performance Control

8.2.1 Enhanced Intel SpeedStep Technology (EIST)

The operating system can manage and choose P-states using the Enhanced Intel® SpeedStep® Technology. This technology offers several key features, including multiple frequencies and voltage points that optimize performance and power efficiency. These operating points are referred to as P-states, and frequency selection is software-controlled by writing to processor model-specific registers (MSRs). The voltage is adjusted based on the selected frequency and the number of active IA cores. Once established, the phase locked loop (PLL) locks onto the target frequency, which is shared by all active IA cores with the same voltage.

In a multi-core processor, the highest frequency P-state requested by any active IA core is selected. Software-requested transitions are permitted at any time, but if a previous transition is in progress, the new transition is deferred until the previous one is completed. The processor internally controls voltage ramp rates to ensure smooth transitions without glitches.

8.2.2 Intel Speed Shift Technology

Intel® Speed Shift Technology is an energy-saving approach to frequency control that relies on hardware rather than operating system control. The operating system is informed of the hardware P-states that are available and can either request a specific P-state or allow the hardware to determine the P-state.

The request made by the operating system is based on the workload requirements and knowledge of the processor's capabilities. Meanwhile, the processor's decision is influenced by various system constraints, such as workload demand, thermal limits, and the minimum and maximum levels of performance requested by the operating system, while taking into account the activity window.

8.2.3 Intel Turbo Boost Technology 2.0

The IA core/processor graphics core of the processor can automatically run faster than its base frequency, using the Intel® Turbo Boost Technology 2.0. This feature operates within power, temperature, and current limits and optimizes performance for both single-threaded and multi-threaded workloads.

With Intel® Turbo Boost Technology 2.0, the application power is directed more towards Thermal Design Power (TDP). The processor can exceed the TDP by going as high as PL2 for short durations. However, if the cooling solution is not designed accordingly, the system may face performance and thermal issues as more applications will run at the maximum power limit for extended periods. For more information about Intel® Turbo Boost 2.0 Technology visit the Intel® website.

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8.2.4 Intel Performance Hybrid Architecture

The Intel® Performance Hybrid Architecture comprises two core types, namely P-Cores and E-Cores:

- P-Cores refer to performance cores
- E-Cores refer to efficient cores

Both P-Cores and E-Cores utilize the same instruction set and model-specific registers (MSRs). However, when hybrid computing is enabled, the available instruction sets are fewer than those available to P-Cores. The processor algorithm determines the frequency of both P-Cores and E-Cores to optimize performance and power usage. The Intel® Performance Hybrid Architecture architecture is optimized for a wide range of workload types, including:

- single threaded
- partially threaded
- multi threaded

For more information about Intel® Performance Hybrid Architecture, refer to the Intel® website:

https://www.intel.com/content/www/us/en/developer/articles/technical/hybrid-architecture.html

8.3 Intel® Virtualization Technology

Intel® Virtualization Technology (Intel® VT) makes a single system appear as multiple independent systems to software. With this technology, multiple, independent operating systems can run simultaneously on a single system. The technology components support virtualization of platforms based on Intel® architecture microprocessors and chipsets. Intel® Virtualization Technology for Intel® 64 and Intel® Architecture (Intel® VT-x) added hardware support in the processor to improve the virtualization performance and robustness.

RTS Real-Time Hypervisor supports Intel® VT and is verified on all current congatec x86 hardware.

Note

congatec supports RTS Hypervisor.

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8.4 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system's thermal management. This results in the operating system having the ability to implement cooling decisions according to the demands of the application.

The conga-HPC/cRLP offers hardware-based support for passive and active cooling. Passive cooling is implemented in the Intel CPU via the Thermal Control Circuit (TCC) Activation Offset setting in the CPU configuration setup sub-menu. The TCC in the processor is activated at 100°C by default but can be lowered by the Activation Offset—for example, an activation offset of "10" will activate TCC at 90°C. ACPI OS support is not required. See section 8.1 "Adaptive Thermal Monitor and Catastrophic Thermal Protection" for more information.

The congatec Board Controller (cBC) supports active cooling solution. The cBC controls the fan's speed based on the temperature readings of the CPU. This feature does not require ACPI OS support. The only software-controlled thermal trip point on conga-HPC/cRLP is the Critical Trip Point. The active or passive cooling policy should ensure that the CPU temperature does not reach this trip point. However, if the critical trip point is reached, the OS will shut down properly in order to prevent damage to the system. Use the "critical trip point" setup node in the BIOS setup menu to determine the temperature threshold at which the system shuts down.

Note

The Automatic Critical Trip Point BIOS setting shuts down the system at 5°C above the maximum specified temperature of the processor.

8.5 ACPI Suspend Modes and Resume Events

The conga-HPC/cRLP BIOS supports S3 (Suspend to RAM), S4 (Suspend to Disk), S5 (Soft-Off) and S5e (congatec proprietary low-power Soft-Off). The table below lists the events that wake the system.

Table 17 Wake Events

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S3-S5; S5e
Onboard LAN Event	Device driver must be configured for Wake On LAN support
SMB_ALERT#	Wakes unconditionally from S3-S5; S5e
PCI Express WAKE#	Wakes unconditionally from S3-S5
WAKE#	Wakes unconditionally from S3
PME#	Activate the wake up capabilities of a PCI device using Windows device manager configuration options for this device or set "Resume On PME#" to "Enabled" in the power setup menu
USB Mouse/Keyboard Event	When "Standby mode" is set to S3, USB hardware must be powered by standby power source. Set "USB Device Wakeup" from S3/S4 to "Enabled" in the ACPI setup menu (if setup node is available in BIOS setup program) In device manager, look for the keyboard/mouse devices. Go to the power management tab and check "Allow this device to bring the computer out of standby".
RTC Alarm	Activate and configure "Resume On RTC Alarm" in the power setup menu (only available in S5)
Watchdog Power Button Event	Wakes unconditionally from S3-S5

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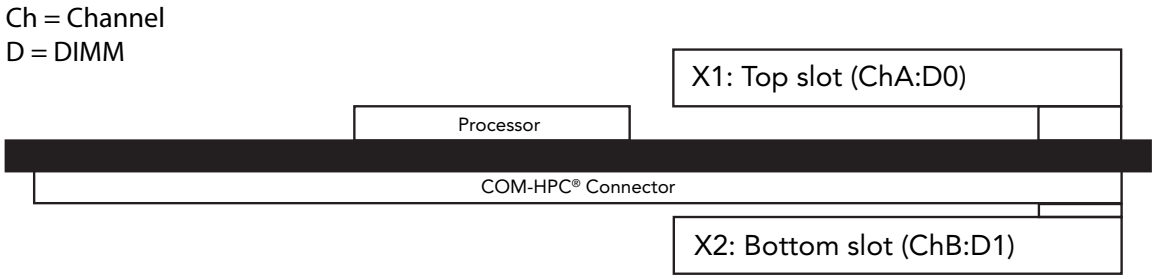
8.6 Memory Population Rules

The diagram below shows the location of the two SO-DIMM memory slots (X1 and X2) on the conga-HPC/cRLP:



The following population rules must be observed:

- Either X1 or X2 must be populated or the system will not boot (POST code 55)
- Populated memory modules should have the same part number for optimal performance and to avoid potential issues

Note

1. *For information about the supported memory of each conga-HPC/cRLP variant, see section 1.3 "Options Information".*
2. *For a list of memory modules offered by congatec, refer to the latest conga-HPC/cRLP datasheet available on the congatec website or contact your congatec sales representative.*

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9 Signal Descriptions and Pinout Tables

This section describes the signals found on the conga-HPC/cRLP. The pinout complies with PICMG® COM-HPC®, revision 1.20. The table below describes the terminology used in this section. The PU/PD column indicates if a pull-up or pull-down resistor has been used. If the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented by congatec.

The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

Note

The Signal Description tables do not list internal pull-ups or pull-downs implemented by the chip vendors. Only pull-ups or pull-downs implemented by congatec are listed. For information about the internal pull-ups or pull-downs implemented by the chip vendors, refer to the respective chip's datasheet.

Table 18 Signal Description Terminology

Term	Description
PU	congatec implemented pull-up resistor
PD	congatec implemented pull-down resistor
T	Higher voltage tolerance
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
I/O 3.3VSB	Input 3.3V tolerant active in standby state
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
OD	Open drain output
V_{OL}	Output low voltage
V_{OH}	Output high voltage
P	Power Input/Output
DDC	Display Data Channel
PCIE	PCI Express®
SATA	Serial ATA
REF	Reference voltage output. May be sourced from a module power plane.
KR	10GBASE-KR compatible signal
PDS	Pull-down strap. A module output pin that is either tied to GND or is not connected. Used to signal module capabilities (pinout type) to the Carrier Board.

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9.1 Connector Signal Descriptions

Table 19 Primary Connector (J1) Pinout

Pin	Row A	Pin	Row B	Pin	Row C	Pin	Row D
A01	VCC	B01	VCC	C01	VCC	D01	VCC
A02	VCC	B02	PWRBTN#	C02	RSTBTN#	D02	VCC
A03	VCC	B03	VCC	C03	VCC	D03	VCC
A04	VCC	B04	THERMTRIP#	C04	CARRIER_HOT#	D04	VCC
A05	VCC	B05	VCC	C05	VCC	D05	VCC
A06	VCC	B06	TAMPER#	C06	VIN_PWROK	D06	VCC
A07	VCC	B07	VCC	C07	VCC	D07	VCC
A08	VCC	B08	SUS_S3#	C08	SUS_S4_S5#	D08	VCC
A09	VCC	B09	VCC	C09	VCC	D09	VCC
A10	GND	B10	WD_STROBE#	C10	GND	D10	WAKE0#
A11	BATLOW#	B11	WD_OUT	C11	FAN_PWMOUT	D11	WAKE1#
A12	PLTRST#	B12	GND	C12	FAN_TACHIN	D12	GND
A13	GND	B13	USB5-	C13	GND	D13	USB1-
A14	USB7-	B14	USB5+	C14	USB3-	D14	USB1+
A15	USB7+	B15	GND	C15	USB3+	D15	GND
A16	GND	B16	USB4-	C16	GND	D16	USB0-
A17	USB6-	B17	USB4+	C17	USB2-	D17	USB0+
A18	USB6+	B18	GND	C18	USB2+	D18	GND
A19	GND	B19	I2S_LRCLK [2]/SNDW_CLK3 [2]/HDA_SYNC	C19	GND	D19	DDI0_SDA_AUX-
A20	DDI1_SDA_AUX-	B20	I2S_DOUT [2]/SNDW_DAT3 [2]/HDA_SDOUT [3]	C20	SNDW_DMIC_CLK1 [2]	D20	DDI0_SCL_AUX+
A21	DDI1_SCL_AUX+	B21	I2S_MCLK [2]/HDA_RST#	C21	SNDW_DMIC_DAT1 [2]	D21	GND
A22	GND	B22	I2S_DIN [2]/SNDW_DAT2 [2]/HDA_SDIN	C22	GND	D22	DDI0_PAIR0-
A23	DDI1_PAIR0-	B23	I2S_CLK [2]/SNDW_CLK2 [2]/HDA_BITCLK	C23	SNDW_DMIC_CLK0 [2]	D23	DDI0_PAIR0+
A24	DDI1_PAIR0+	B24	VCC_5V_SBY	C24	SNDW_DMIC_DAT0 [2]	D24	GND
A25	GND	B25	USB67_OC#	C25	GND	D25	DDI0_PAIR1-
A26	DDI1_PAIR1-	B26	USB45_OC#	C26	DDI0_DDC_AUX_SEL	D26	DDI0_PAIR1+
A27	DDI1_PAIR1+	B27	USB23_OC#	C27	DDI1_DDC_AUX_SEL	D27	GND
A28	GND	B28	USB01_OC#	C28	DDI0_HPD	D28	DDI0_PAIR2-
A29	DDI1_PAIR2-	B29	SML1_CLK	C29	DDI1_HPD	D29	DDI0_PAIR2+
A30	DDI1_PAIR2+	B30	SML1_DAT	C30	eDP_HPD	D30	GND
A31	GND	B31	PMCALERT#	C31	eDP_VDD_EN	D31	DDI0_PAIR3-
A32	DDI1_PAIR3-	B32	SML0_CLK	C32	eDP_BKLT_EN	D32	DDI0_PAIR3+
A33	DDI1_PAIR3+	B33	SML0_DAT	C33	eDP_BKLTCTL	D33	GND
A34	GND	B34	USB_PD_ALERT#	C34	GND	D34	AC_PRESENT
A35	eDP_AUX-	B35	USB_PD_I2C_CLK	C35	USB1_AUX-	D35	RSVD
A36	eDP_AUX+	B36	USB_PD_I2C_DAT	C36	USB1_AUX+	D36	GND

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A37	GND	B37	USB_RT_ENA	C37	GND	D37	USB1_SSTX0-
A38	eDP_TX0-	B38	USB1_LSRX	C38	USB1_SSRX0-	D38	USB1_SSTX0+
A39	eDP_TX0+	B39	USB1_LSTX	C39	USB1_SSRX0+	D39	GND
A40	GND	B40	USB0_LSRX	C40	GND	D40	USB1_SSTX1-
A41	eDP_TX1-	B41	USB0_LSTX	C41	USB1_SSRX1-	D41	USB1_SSTX1+
A42	eDP_TX1+	B42	GND	C42	USB1_SSRX1+	D42	GND
A43	GND	B43	USB0_AUX-	C43	GND	D43	USB0_SSTX0-
A44	eDP_TX2-	B44	USB0_AUX+	C44	USB0_SSRX0-	D44	USB0_SSTX0+
A45	eDP_TX2+	B45	LID#	C45	USB0_SSRX0+	D45	GND
A46	GND	B46	SLEEP#	C46	GND	D46	USB0_SSTX1-
A47	eDP_TX3-	B47	VCC_BOOT_SPI (3.3V)	C47	USB0_SSRX1-	D47	USB0_SSTX1+
A48	eDP_TX3+	B48	BOOT_SPI_CS#	C48	USB0_SSRX1+	D48	GND
A49	GND	B49	BSEL0	C49	GND	D49	SATA0_RX-
A50	eSPI_IO0	B50	BSEL1	C50	BOOT_SPI_IO0	D50	SATA0_RX+
A51	eSPI_IO1	B51	BSEL2	C51	BOOT_SPI_IO1	D51	GND
A52	eSPI_IO2	B52	eSPI_ALERT0#	C52	BOOT_SPI_IO2 [3]	D52	SATA0_TX-
A53	eSPI_IO3	B53	eSPI_ALERT1# [2]	C53	BOOT_SPI_IO3 [3]	D53	SATA0_TX+
A54	eSPI_CLK	B54	eSPI_CS0#	C54	BOOT_SPI_CLK	D54	GND
A55	GND	B55	eSPI_CS1# [2]	C55	GND	D55	SATA1_RX-
A56	PCIe_CLKREQ0_LO#	B56	eSPI_RST#	C56	PCIe_REFCLK0_HI-	D56	SATA1_RX+
A57	PCIe_CLKREQ0_HI#	B57	GND	C57	PCIe_REFCLK0_HI+	D57	GND
A58	GND	B58	PCIe_BMC_RX- [1]	C58	GND	D58	SATA1_TX-
A59	PCIe_BMC_TX- [1]	B59	PCIe_BMC_RX+ [1]	C59	PCIe_REFCLK0_LO-	D59	SATA1_TX+
A60	PCIe_BMC_TX+ [1]	B60	GND	C60	PCIe_REFCLK0_LO+	D60	GND
A61	GND	B61	PCIe08_RX-	C61	GND	D61	PCIe00_TX-
A62	PCIe08_TX-	B62	PCIe08_RX+	C62	PCIe00_RX-	D62	PCIe00_TX+
A63	PCIe08_TX+	B63	GND	C63	PCIe00_RX+	D63	GND
A64	GND	B64	PCIe09_RX-	C64	GND	D64	PCIe01_TX-
A65	PCIe09_TX-	B65	PCIe09_RX+	C65	PCIe01_RX-	D65	PCIe01_TX+
A66	PCIe09_TX+	B66	GND	C66	PCIe01_RX+	D66	GND
A67	GND	B67	PCIe10_RX-	C67	GND	D67	PCIe02_TX-
A68	PCIe10_TX-	B68	PCIe10_RX+	C68	PCIe02_RX-	D68	PCIe02_TX+
A69	PCIe10_TX+	B69	GND	C69	PCIe02_RX+	D69	GND
A70	GND	B70	PCIe11_RX-	C70	GND	D70	PCIe03_TX-
A71	PCIe11_TX-	B71	PCIe11_RX+	C71	PCIe03_RX-	D71	PCIe03_TX+
A72	PCIe11_TX+	B72	GND	C72	PCIe03_RX+	D72	GND
A73	GND	B73	PCIe12_RX-	C73	GND	D73	PCIe04_TX-
A74	PCIe12_TX-	B74	PCIe12_RX+	C74	PCIe04_RX-	D74	PCIe04_TX+
A75	PCIe12_TX+	B75	GND	C75	PCIe04_RX+	D75	GND
A76	GND	B76	PCIe13_RX-	C76	GND	D76	PCIe05_TX-
A77	PCIe13_TX-	B77	PCIe13_RX+	C77	PCIe05_RX-	D77	PCIe05_TX+
A78	PCIe13_TX+	B78	GND	C78	PCIe05_RX+	D78	GND

A79	GND	B79	PCIe14_RX-	C79	GND	D79	PCIe06_TX-
A80	PCIe14_TX-	B80	PCIe14_RX+	C80	PCIe06_RX-	D80	PCIe06_TX+
A81	PCIe14_TX+	B81	GND	C81	PCIe06_RX+	D81	GND
A82	GND	B82	PCIe15_RX-	C82	GND	D82	PCIe07_TX-
A83	PCIe15_TX-	B83	PCIe15_RX+	C83	PCIe07_RX-	D83	PCIe07_TX+
A84	PCIe15_TX+	B84	GND	C84	PCIe07_RX+	D84	GND
A85	GND	B85	TEST#	C85	GND	D85	NBASET0_MDI0-
A86	VCC_RTC	B86	RSMRST_OUT#	C86	SMB_CLK	D86	NBASET0_MDI0+
A87	SUS_CLK	B87	UART1_TX	C87	SMB_DAT	D87	GND
A88	GPIO_00	B88	UART1_RX	C88	SMB_ALERT#	D88	NBASET0_MDI1-
A89	GPIO_01	B89	UART1_RTS#	C89	UART0_TX	D89	NBASET0_MDI1+
A90	GPIO_02	B90	UART1_CTS#	C90	UART0_RX	D90	GND
A91	GPIO_03	B91	IPMB_CLK	C91	UART0_RTS#	D91	NBASET0_MDI2-
A92	GPIO_04	B92	IPMB_DAT	C92	UART0_CTS#	D92	NBASET0_MDI2+
A93	GPIO_05	B93	GP_SPI_MOSI	C93	I2C0_CLK	D93	GND
A94	GPIO_06	B94	GP_SPI_MISO	C94	I2C0_DAT	D94	NBASET0_MDI3-
A95	GPIO_07	B95	GP_SPI_CS0#	C95	I2C0_ALERT#	D95	NBASET0_MDI3+
A96	GPIO_08	B96	GP_SPI_CS1#	C96	I2C1_CLK [2]	D96	GND
A97	GPIO_09	B97	GP_SPI_CS2#	C97	I2C1_DAT [2]	D97	NBASET0_LINK_MAX#
A98	GPIO_10	B98	GP_SPI_CS3#	C98	NBASET0_SDP	D98	NBASET0_LINK_MID#
A99	GPIO_11	B99	GP_SPI_CLK	C99	NBASET0_CTREF [1]	D99	NBASET0_LINK_ACT#
A100	TYPE0 [1]	B100	GP_SPI_ALERT#	C100	TYPE1	D100	TYPE2

Note

1. *Not connected*
2. *Not supported*
3. *Boot strap signal*

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Table 20 Secondary Connector (J2) Pinout

Pin	Row E	Pin	Row F	Pin	Row G	Pin	Row H
E1	RAPID_SHUTDOWN	F1	FUSA_STATUS0 [1]	G1	VCC_5V_SBY	H1	GND
E2	GND	F2	FUSA_STATUS1 [1]	G2	GND	H2	USB2_SSTX0-
E3	DDI2_SDA_AUX-	F3	FUSA_ALERT# [1]	G3	USB2_SSRX0-	H3	USB2_SSTX0+
E4	DDI2_SCL_AUX+	F4	FUSA_SPI_CS# [2]	G4	USB2_SSRX0+	H4	GND
E5	GND	F5	FUSA_SPI_CLK [2]	G5	GND	H5	USB2_SSTX1- [1]
E6	DDI2_PAIR0-	F6	FUSA_SPI_MISO [1]	G6	USB2_SSRX1- [1]	H6	USB2_SSTX1+ [1]
E7	DDI2_PAIR0+	F7	FUSA_SPI_MOSI [2]	G7	USB2_SSRX1+ [1]	H7	GND
E8	GND	F8	FUSA_SPI_ALERT [1]	G8	GND	H8	USB3_SSTX0-
E9	DDI2_PAIR1-	F9	FUSA_VOLTAGE_ERR# [1]	G9	USB3_SSRX0-	H9	USB3_SSTX0+
E10	DDI2_PAIR1+	F10	PROCHOT#	G10	USB3_SSRX0+	H10	GND
E11	GND	F11	CATERR#	G11	GND	H11	USB3_SSTX1- [1]
E12	DDI2_PAIR2-	F12	RSVD	G12	USB3_SSRX1- [1]	H12	USB3_SSTX1+ [1]
E13	DDI2_PAIR2+	F13	RSVD	G13	USB3_SSRX1+ [1]	H13	GND
E14	GND	F14	RSVD	G14	GND	H14	USB2_AUX- [1]
E15	DDI2_PAIR3-	F15	RSVD	G15	USB3_LSRX	H15	USB2_AUX+ [1]
E16	DDI2_PAIR3+	F16	RSVD	G16	USB3_LSTX	H16	GND
E17	GND	F17	RSVD	G17	USB2_LSRX	H17	USB3_AUX- [1]
E18	DDI2_DDC_AUX_SEL	F18	RSVD	G18	USB2_LSTX	H18	USB3_AUX+ [1]
E19	DDI2_HPD	F19	GND	G19	PEG_LANE_REV#	H19	GND
E20	GND	F20	PCIe32_RX- [1]	G20	GND	H20	PCIe40_TX- [1]
E21	PCIe32_TX- [1]	F21	PCIe32_RX+ [1]	G21	PCIe40_RX- [1]	H21	PCIe40_TX+ [1]
E22	PCIe32_TX+ [1]	F22	GND	G22	PCIe40_RX+ [1]	H22	GND
E23	GND	F23	PCIe33_RX- [1]	G23	GND	H23	PCIe41_TX- [1]
E24	PCIe33_TX- [1]	F24	PCIe33_RX+ [1]	G24	PCIe41_RX- [1]	H24	PCIe41_TX+ [1]
E25	PCIe33_TX+ [1]	F25	GND	G25	PCIe41_RX+ [1]	H25	GND
E26	GND	F26	PCIe34_RX- [1]	G26	GND	H26	PCIe42_TX- [1]
E27	PCIe34_TX- [1]	F27	PCIe34_RX+ [1]	G27	PCIe42_RX- [1]	H27	PCIe42_TX+ [1]
E28	PCIe34_TX+ [1]	F28	GND	G28	PCIe42_RX+ [1]	H28	GND
E29	GND	F29	PCIe35_RX- [1]	G29	GND	H29	PCIe43_TX- [1]
E30	PCIe35_TX- [1]	F30	PCIe35_RX+ [1]	G30	PCIe43_RX- [1]	H30	PCIe43_TX+ [1]
E31	PCIe35_TX+ [1]	F31	GND	G31	PCIe43_RX+ [1]	H31	GND
E32	GND	F32	PCIe36_RX- [1]	G32	GND	H32	PCIe44_TX- [1]
E33	PCIe36_TX- [1]	F33	PCIe36_RX+ [1]	G33	PCIe44_RX- [1]	H33	PCIe44_TX+ [1]
E34	PCIe36_TX+ [1]	F34	GND	G34	PCIe44_RX+ [1]	H34	GND
E35	GND	F35	PCIe37_RX- [1]	G35	GND	H35	PCIe45_TX- [1]
E36	PCIe37_TX- [1]	F36	PCIe37_RX+ [1]	G36	PCIe45_RX- [1]	H36	PCIe45_TX+ [1]
E37	PCIe37_TX+ [1]	F37	GND	G37	PCIe45_RX+ [1]	H37	GND
E38	GND	F38	PCIe38_RX- [1]	G38	GND	H38	PCIe46_TX- [1]

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E39	PCIe38_TX- [1]	F39	PCIe38_RX+ [1]	G39	PCIe46_RX- [1]	H39	PCIe46_TX+ [1]
E40	PCIe38_TX+ [1]	F40	GND	G40	PCIe46_RX+ [1]	H40	GND
E41	GND	F41	PCIe39_RX- [1]	G41	GND	H41	PCIe47_TX- [1]
E42	PCIe39_TX- [1]	F42	PCIe39_RX+ [1]	G42	PCIe47_RX- [1]	H42	PCIe47_TX+ [1]
E43	PCIe39_TX+ [1]	F43	GND	G43	PCIe47_RX+ [1]	H43	GND
E44	GND	F44	PCIe16_RX- [4]	G44	GND	H44	PCIe24_TX- [1]
E45	PCIe16_TX- [4]	F45	PCIe16_RX+ [4]	G45	PCIe24_RX- [1]	H45	PCIe24_TX+ [1]
E46	PCIe16_TX+ [4]	F46	GND	G46	PCIe24_RX+ [1]	H46	GND
E47	GND	F47	PCIe17_RX- [4]	G47	GND	H47	PCIe25_TX- [1]
E48	PCIe17_TX- [4]	F48	PCIe17_RX+ [4]	G48	PCIe25_RX- [1]	H48	PCIe25_TX+ [1]
E49	PCIe17_TX+ [4]	F49	GND	G49	PCIe25_RX+ [1]	H49	GND
E50	GND	F50	PCIe18_RX- [4]	G50	GND	H50	PCIe26_TX- [1]
E51	PCIe18_TX- [4]	F51	PCIe18_RX+ [4]	G51	PCIe26_RX- [1]	H51	PCIe26_TX+ [1]
E52	PCIe18_TX+ [4]	F52	GND	G52	PCIe26_RX+ [1]	H52	GND
E53	GND	F53	PCIe19_RX- [4]	G53	GND	H53	PCIe27_TX- [1]
E54	PCIe19_TX- [4]	F54	PCIe19_RX+ [4]	G54	PCIe27_RX- [1]	H54	PCIe27_TX+ [1]
E55	PCIe19_TX+ [4]	F55	GND	G55	PCIe27_RX+ [1]	H55	GND
E56	GND	F56	PCIe20_RX- [4]	G56	GND	H56	PCIe28_TX- [1]
E57	PCIe20_TX- [4]	F57	PCIe20_RX+ [4]	G57	PCIe28_RX- [1]	H57	PCIe28_TX+ [1]
E58	PCIe20_TX+ [4]	F58	GND	G58	PCIe28_RX+ [1]	H58	GND
E59	GND	F59	PCIe21_RX- [4]	G59	GND	H59	PCIe29_TX- [1]
E60	PCIe21_TX- [4]	F60	PCIe21_RX+ [4]	G60	PCIe29_RX- [1]	H60	PCIe29_TX+ [1]
E61	PCIe21_TX+ [4]	F61	GND	G61	PCIe29_RX+ [1]	H61	GND
E62	GND	F62	PCIe22_RX- [4]	G62	GND	H62	PCIe30_TX- [1]
E63	PCIe22_TX- [4]	F63	PCIe22_RX+ [4]	G63	PCIe30_RX- [1]	H63	PCIe30_TX+ [1]
E64	PCIe22_TX+ [4]	F64	GND	G64	PCIe30_RX+ [1]	H64	GND
E65	GND	F65	PCIe23_RX- [4]	G65	GND	H65	PCIe31_TX- [1]
E66	PCIe23_TX- [4]	F66	PCIe23_RX+ [4]	G66	PCIe31_RX- [1]	H66	PCIe31_TX+ [1]
E67	PCIe23_TX+ [4]	F67	GND	G67	PCIe31_RX+ [1]	H67	GND
E68	GND	F68	RSVD	G68	GND	H68	RSVD
E69	RSVD	F69	RSVD	G69	RSVD	H69	RSVD
E70	RSVD	F70	GND	G70	RSVD	H70	GND
E71	RSVD	F71	NBASET1_MDI0-	G71	GND	H71	CSI1_RX0- [2]
E72	RSVD	F72	NBASET1_MDI0+	G72	CSI0_RX0- [2]	H72	CSI1_RX0+ [2]
E73	RSVD	F73	GND	G73	CSI0_RX0+ [2]	H73	GND
E74	RSVD	F74	NBASET1_MDI1-	G74	GND	H74	CSI1_RX1-[2]
E75	RSVD	F75	NBASET1_MDI1+	G75	CSI0_RX1- [2]	H75	CSI1_RX1+ [2]
E76	RSVD	F76	GND	G76	CSI0_RX1+ [2]	H76	GND
E77	RSVD	F77	NBASET1_MDI2-	G77	GND	H77	CSI1_RX2- [2]
E78	NBASET1_CTREF [1]	F78	NBASET1_MDI2+	G78	CSI0_RX2- [2]	H78	CSI1_RX2+ [2]
E79	NBASET1_SDP	F79	GND	G79	CSI0_RX2+ [2]	H79	GND

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E80	NBASET1_LINK_MID#	F80	NBASET1_MDI3-	G80	GND	H80	CSI1_RX3- [2]
E81	NBASET1_LINK_ACT#	F81	NBASET1_MDI3+	G81	CSI0_RX3- [2]	H81	CSI1_RX3+ [2]
E82	NBASET1_LINK_MAX#	F82	GND	G82	CSI0_RX3+ [2]	H82	GND
E83	GND	F83	RSVD	G83	GND	H83	CSI1_CLK- [2]
E84	RSVD	F84	RSVD	G84	CSI0_CLK- [2]	H84	CSI1_CLK+ [2]
E85	RSVD	F85	GND	G85	CSI0_CLK+ [2]	H85	GND
E86	GND	F86	ETH0_TX- [1]	G86	GND	H86	CSI1_I2C_CLK [2]
E87	ETH0_RX- [1]	F87	ETH0_TX+ [1]	G87	CSI0_I2C_CLK [2]	H87	CSI1_I2C_DAT [2]
E88	ETH0_RX+ [1]	F88	GND	G88	CSI0_I2C_DAT [2]	H88	CSI1_MCLK [2]
E89	GND	F89	ETH1_TX- [1]	G89	CSI0_MCLK	H89	CSI1_RST# [2]
E90	ETH1_RX- [1]	F90	ETH1_TX+ [1]	G90	CSI0_RST# [2]	H90	CSI1_ENA [2]
E91	ETH1_RX+ [1]	F91	GND	G91	CSI0_ENA [2]	H91	GND
E92	GND	F92	PCIe_REFCLK2-	G92	GND	H92	PCIe_REFCLKIN0- [1]
E93	PCIe_REFCLK1-	F93	PCIe_REFCLK2+	G93	RSVD	H93	PCIe_REFCLKIN0+ [1]
E94	PCIe_REFCLK1+	F94	GND	G94	RSVD	H94	GND
E95	GND	F95	RSVD	G95	GND	H95	PCIe_REFCLKIN1- [1]
E96	PCIe_CLKREQ1#	F96	ETH0-1_PRSNT# [2]	G96	ETH0-1_I2C_CLK [2]	H96	PCIe_REFCLKIN1+ [1]
E97	PCIe_CLKREQ2#	F97	ETH0-1_PHY_RST# [2]	G97	ETH0-1_I2C_DAT [2]	H97	GND
E98	PCIe_CLKREQ_OUT0# [1]	F98	ETH0_SDP [1]	G98	ETH0-1_PHY_INT# [2]	H98	ETH0-1_MDIO_CLK [1]
E99	PCIe_CLKREQ_OUT1# [1]	F99	ETH1_SDP [1]	G99	ETH0-1_INT# [2]	H99	ETH0-1_MDIO_DAT [2]
E100	PCIe_PERST_IN0# [2]	F100	PCIe_PERST_IN1# [2]	G100	PCIe_WAKE_OUT0# [1]	H100	PCIe_WAKE_OUT1# [1]

Note

1. *Not connected*
2. *Not supported*
3. *Boot strap signal*
4. *H-Series CPUs only*

Table 21 NBASE-T Ethernet Signal Descriptions

<table>
<tr><th>Gigabit Ethernet</th><th>Pin #</th><th>Description</th><th>I/O</th><th>PU/PD</th><th>Comment</th></tr>
<tr><td>NBASET0_MDI0+
NBASET0_MDI0-
NBASET0_MDI1+
NBASET0_MDI1-
NBASET0_MDI2+
NBASET0_MDI2-
NBASET0_MDI3+
NBASET0_MDI3-

NBASET1_MDI0+
NBASET1_MDI0-
NBASET1_MDI1+
NBASET1_MDI1-
NBASET1_MDI2+
NBASET1_MDI2-
NBASET1_MDI3+
NBASET1_MDI3-</td><td>D86
D85
D89
D88
D92
D91
D95
D94

F72
F71
F75
F74
F78
F77
F81
F80</td><td>Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 10 Gbps, 1 Gbps, 100 Mbps and 10 Mbps modes.
Some pairs are unused in some modes, per the following:

<table><tr><th></th><th>10000BASE-T
1000BASE-T</th><th>100BASE-TX</th><th>10BASE-T</th></tr><tr><td>MDI[0]+/-</td><td>B1_DA+/-</td><td>TX+/-</td><td>TX+/-</td></tr><tr><td>MDI[1]+/-</td><td>B1_DB+/-</td><td>RX+/-</td><td>RX+/-</td></tr><tr><td>MDI[2]+/-</td><td>B1_DC+/-</td><td></td><td></td></tr><tr><td>MDI[3]+/-</td><td>B1_DD+/-</td><td></td><td></td></tr></table></td><td>I/O MDI
3.3 VSB</td><td></td><td>The conga-HPC/cRLP supports up to 2.5 Gbps.</td></tr>
<tr><td>NBASET0_LINK_ACT#
NBASET1_LINK_ACT#</td><td>D99
E81</td><td>NBASE-T Ethernet Controller activity indicator, active low.
20 mA or more current sink capability at V_{OL} of 0.4V max.
20 mA or more current source capability at V_{OH} of 2.4V min.</td><td>O 3.3 VSB</td><td></td><td></td></tr>
<tr><td>NBASET0_LINK_MAX#
NBASET1_LINK_MAX#</td><td>D97
E82</td><td>NBASE-T Ethernet Controller MAX Speed Link indicator, active low. If active, the link is established at the maximum speed that the Ethernet controller is capable of (which may be 10G, 5G, 2.5G etc).
20 mA or more current sink capability at V_{OL} of 0.4V max.
20 mA or more current source capability at V_{OH} of 2.4V min.</td><td>O 3.3 VSB</td><td></td><td>The conga-HPC/cRLP supports up to 2.5 Gbps.</td></tr>
<tr><td>NBASET0_LINK_MID#
NBASET1_LINK_MID#</td><td>D98
E80</td><td>NBASE-T Ethernet Controller MID Speed Link indicator, active low. If active, the link is established but at a speed lower than what the maximum speed that the Ethernet controller is capable of.
20 mA or more current sink capability at V_{OL} of 0.4V max.
20 mA or more current source capability at V_{OH} of 2.4V min.</td><td>O 3.3 VSB</td><td></td><td></td></tr>
<tr><td>NBASET0_CTREF
NBASET1_CTREF</td><td>C99
E78</td><td>Reference voltage for Carrier Board NBASET Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the Module PHY and may be as low as 0V and as high as 3.3V.

If not needed, these pins may be left open on the Carrier. The reference voltage output shall be current limited on the Module. In the case in which the reference is shorted to ground, the current shall be limited to 250 mA or less.</td><td>REF</td><td></td><td>Not connected</td></tr>
<tr><td>NBASET0_SDP
NBASET1_SDP</td><td>C98
E79</td><td>NBASE-T Ethernet Controller 0 Software-Definable Pin. Can also be used for IEEE1588 support such as a 1pps signal.</td><td>I/O 3.3 VSB</td><td></td><td></td></tr>
</table>

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Table 22 Ethernet KR and KX Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
ETH0_TX+ ETH0_TX-	F87 F86	Ethernet KR ports, transmit output differential pairs.	O KR		Not connected
ETH0_RX+ ETH0_RX-	E88 E87	Ethernet KR ports, receive input differential pairs.	I KR		
ETH1_TX+ ETH1_TX-	F90 F89	Ethernet KR ports, transmit output differential pairs.	O KR		Not connected
ETH1_RX+ ETH1_RX-	E91 E90	Ethernet KR ports, receive input differential pairs.	I KR		
ETH0-1_MDIO_DAT	H99	Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY for ETHx ports 0 to 1.	I/O 3.3 V	PU 2.2 KΩ 3.3 VSB	Not supported
ETH0-1_MDIO_CLK	H98	Clock signal for Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY for ETHx ports 0 to 1.	O 3.3 V		Not connected
ETH0-1_INT#	G99	Active low interrupt signal from IO Port expanders for ETH ports 0 to 1.	I 3.3 V	PU 2.2 KΩ 3.3 VSB	Not supported
ETH0-1_PHY_INT#	G98	Active low PHY interrupt signal from ETH ports 0 to 1.	I 3.3 V	PU 2.2 KΩ 3.3 VSB	
ETH0-1_PHY_RST#	F97	Active low output PHY reset signal for ETH ports 0 to 1.	O 3.3 V	PD 0 RΩ	
ETH0-1_I2C_DAT	G97	I2C data signal of the 2-wire management interface used by the Ethernet KR controller to access the management registers of an external SFP Module or to configure the Carrier PHY for ETHx ports 0 to 3 (Server) or 0 to 1 (Client) and for serialized status information (e.g. LED states).	I/O OD 3.3 V	PU 2.2 KΩ 3.3 VSB	
ETH0-1_I2C_CLK	G96	The I2C clock signals associated with ETH0-3 I2C data lines in the row above.	I/O OD 3.3 V	PU 2.2 KΩ 3.3 VSB	
ETH0_SDP ETH1_SDP	F98 F99	Software-Definable Pins. Can also be used for IEEE1588 support such as a PPS signal.	I/O 3.3 V		Not connected
ETH0-1_PRSNT#	F96	Carrier pulls this line to GND if there is Carrier hardware present to support Ethernet KR signaling on ETH0 or ETH1. If only one KR channel is supported, it should be on ETH0.	I 3.3 V	PU 2.2 KΩ 3.3 VSB	Not supported

Note

The conga-HPC/cRLP does not support Ethernet KR and KX interfaces.

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Table 23 SATA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_TX+ SATA0_TX-	D53 D52	Serial ATA channel 0, Transmit Output differential pair.	O SATA		Either SATA0 (default) or PCIe02 is supported (BIOS Setup option).
SATA0_RX+ SATA0_RX-	D50 D49	Serial ATA channel 0, Receive Input differential pair.	I SATA		
SATA1_TX+ SATA1_TX-	D59 D58	Serial ATA channel 1, Transmit Output differential pair.	O SATA		Either SATA1 (default) or PCIe03 (BIOS Setup option) or optional onboard NVMe SSD is supported.
SATA1_RX+ SATA1_RX-	D56 D55	Serial ATA channel 1, Receive Input differential pair.	I SATA		

Table 24 PCI Express Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIe00_TX+ PCIe00_TX-	D62 D61	PCI Express Transmit Output Differential Pairs 0	O PCIE		PCIe Gen 3
PCIe00_RX+ PCIe00_RX-	C63 C62	PCI Express Receive Input Differential Pairs 0	I PCIE		PCIe Gen 3
PCIe01_TX+ PCIe01_TX-	D65 D64	PCI Express Transmit Output Differential Pairs 1	O PCIE		PCIe Gen 3
PCIe01_RX+ PCIe01_RX-	C66 C65	PCI Express Receive Input Differential Pairs 1	I PCIE		PCIe Gen 3
PCIe02_TX+ PCIe02_TX-	D68 D67	PCI Express Transmit Output Differential Pairs 2	O PCIE		PCIe Gen 3 Either SATA0 (default) or PCIe02 is supported (BIOS Setup option).
PCIe02_RX+ PCIe02_RX-	C69 C68	PCI Express Receive Input Differential Pairs 2	I PCIE		
PCIe03_TX+ PCIe03_TX-	D71 D70	PCI Express Transmit Output Differential Pairs 3	O PCIE		PCIe Gen 3 Either SATA1 (default) or PCIe03 (BIOS Setup option) or optional onboard NVMe SSD is supported.
PCIe03_RX+ PCIe03_RX-	C72 C71	PCI Express Receive Input Differential Pairs 3	I PCIE		
PCIe04_TX+ PCIe04_TX-	D74 D73	PCI Express Transmit Output Differential Pairs 4	O PCIE		PCIe Gen 3
PCIe04_RX+ PCIe04_RX-	C75 C74	PCI Express Receive Input Differential Pairs 4	I PCIE		PCIe Gen 3
PCIe05_TX+ PCIe05_TX-	D77 D76	PCI Express Transmit Output Differential Pairs 5	O PCIE		PCIe Gen 3
PCIe05_RX+ PCIe05_RX-	C78 C77	PCI Express Receive Input Differential Pairs 5	I PCIE		PCIe Gen 3
PCIe06_TX+ PCIe06_TX-	D80 D79	PCI Express Transmit Output Differential Pairs 6	O PCIE		PCIe Gen 3

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PCIe06_RX+ PCIe06_RX-	C81 C80	PCI Express Receive Input Differential Pairs 6	I PCIE		PCIe Gen 3
PCIe07_TX+ PCIe07_TX-	D83 D82	PCI Express Transmit Output Differential Pairs 7	O PCIE		PCIe Gen 3
PCIe07_RX+ PCIe07_RX-	C84 C83	PCI Express Receive Input Differential Pairs 7	I PCIE		PCIe Gen 3
PCIe08_TX+ PCIe08_TX-	A63 A62	PCI Express Transmit Output Differential Pairs 8	O PCIE		PCIe Gen 4
PCIe08_RX+ PCIe08_RX-	B62 B61	PCI Express Receive Input Differential Pairs 8	I PCIE		PCIe Gen 4
PCIe09_TX+ PCIe09_TX-	A66 A65	PCI Express Transmit Output Differential Pairs 9	O PCIE		PCIe Gen 4
PCIe09_RX+ PCIe09_RX-	B65 B64	PCI Express Receive Input Differential Pairs 9	I PCIE		PCIe Gen 4
PCIe10_TX+ PCIe10_TX-	A69 A68	PCI Express Transmit Output Differential Pairs 10	O PCIE		PCIe Gen 4
PCIE10_RX+ PCIE10_RX-	B68 B67	PCI Express Receive Input Differential Pairs 10	I PCIE		PCIe Gen 4
PCIE11_TX+ PCIE11_TX-	A72 A71	PCI Express Transmit Output Differential Pairs 11	O PCIE		PCIe Gen 4
PCIE11_RX+ PCIE11_RX-	B71 B70	PCI Express Receive Input Differential Pairs 11	I PCIE		PCIe Gen 4
PCIE12_TX+ PCIE12_TX-	B75 A74	PCI Express Transmit Output Differential Pairs 12	O PCIE		PCIe Gen 4
PCIE12_RX+ PCIE12_RX-	B74 B73	PCI Express Receive Input Differential Pairs 12	I PCIE		PCIe Gen 4
PCIE13_TX+ PCIE13_TX-	A78 A77	PCI Express Transmit Output Differential Pairs 13	O PCIE		PCIe Gen 4
PCIE13_RX+ PCIE13_RX-	B77 B76	PCI Express Receive Input Differential Pairs 13	I PCIE		PCIe Gen 4
PCIE14_TX+ PCIE14_TX-	A81 A80	PCI Express Transmit Output Differential Pairs 14	O PCIE		PCIe Gen 4
PCIE14_RX+ PCIE14_RX-	B80 B79	PCI Express Receive Input Differential Pairs 14	I PCIE		PCIe Gen 4
PCIE15_TX+ PCIE15_TX-	A84 A83	PCI Express Transmit Output Differential Pairs 15	O PCIE		PCIe Gen 4
PCIE15_RX+ PCIE15_RX-	B83 B82	PCI Express Receive Input Differential Pairs 15	I PCIE		PCIe Gen 4
PCIE16_TX+ PCIE16_TX-	E46 E45	PCI Express Transmit Output Differential Pairs 16	O PCIE		PCIe Gen 5 H-Series CPUs only
PCIE16_RX+ PCIE16_RX-	F45 F44	PCI Express Receive Input Differential Pairs 16	I PCIE		

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PCIE17_TX+ PCIE17_TX-	E49 E48	PCI Express Transmit Output Differential Pairs 17	O PCIE		PCIe Gen 5 H-Series CPUs only
PCIE17_RX+ PCIE17_RX-	F48 F47	PCI Express Receive Input Differential Pairs 17	I PCIE		
PCIE18_TX+ PCIE18_TX-	E52 E51	PCI Express Transmit Output Differential Pairs 18	O PCIE		PCIe Gen 5 H-Series CPUs only
PCIE18_RX+ PCIE18_RX-	F51 F50	PCI Express Receive Input Differential Pairs 18	I PCIE		
PCIE19_TX+ PCIE19_TX-	E55 E54	PCI Express Transmit Output Differential Pairs 19	O PCIE		PCIe Gen 5 H-Series CPUs only
PCIE19_RX+ PCIE19_RX-	F54 F53	PCI Express Receive Input Differential Pairs 19	I PCIE		
PCIE20_TX+ PCIE20_TX-	E58 E57	PCI Express Transmit Output Differential Pairs 20	O PCIE		PCIe Gen 5 H-Series CPUs only
PCIE20_RX+ PCIE20_RX-	F57 F56	PCI Express Receive Input Differential Pairs 20	I PCIE		
PCIE21_TX+ PCIE21_TX-	E61 E60	PCI Express Transmit Output Differential Pairs 21	O PCIE		PCIe Gen 5 H-Series CPUs only
PCIE21_RX+ PCIE21_RX-	F60 F59	PCI Express Receive Input Differential Pairs 21	I PCIE		
PCIE22_TX+ PCIE22_TX-	E64 E63	PCI Express Transmit Output Differential Pairs 22	O PCIE		PCIe Gen 5 H-Series CPUs only
PCIE22_RX+ PCIE22_RX-	F63 F62	PCI Express Receive Input Differential Pairs 22	I PCIE		
PCIE23_TX+ PCIE23_TX-	E67 E66	PCI Express Transmit Output Differential Pairs 23	O PCIE		PCIe Gen 5 H-Series CPUs only
PCIE23_RX+ PCIE23_RX-	F66 F65	PCI Express Receive Input Differential Pairs 23	I PCIE		
PCIE24_TX+ PCIE24_TX-	H45 H44	PCI Express Transmit Output Differential Pairs 24	O PCIE		Not connected
PCIE24_RX+ PCIE24_RX-	G46 G45	PCI Express Receive Input Differential Pairs 24	I PCIE		
PCIE25_TX+ PCIE25_TX-	H48 H47	PCI Express Transmit Output Differential Pairs 25	O PCIE		Not connected
PCIE25_RX+ PCIE25_RX-	G46 G45	PCI Express Receive Input Differential Pairs 25	I PCIE		
PCIE26_TX+ PCIE26_TX-	H51 H50	PCI Express Transmit Output Differential Pairs 26	O PCIE		Not connected
PCIE26_RX+ PCIE26_RX-	G52 G51	PCI Express Receive Input Differential Pairs 26	I PCIE		
PCIE27_TX+ PCIE27_TX-	H54 H53	PCI Express Transmit Output Differential Pairs 27	O PCIE		Not connected
PCIE27_RX+ PCIE27_RX-	G55 G54	PCI Express Receive Input Differential Pairs 27	I PCIE		

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PCIE28_TX+ PCIE28_TX-	H57 H56	PCI Express Transmit Output Differential Pairs 28	O PCIE		Not connected
PCIE28_RX+ PCIE28_RX-	G58 G57	PCI Express Receive Input Differential Pairs 28	I PCIE		
PCIE29_TX+ PCIE29_TX-	H60 H59	PCI Express Transmit Output Differential Pairs 29	O PCIE		Not connected
PCIE29_RX+ PCIE29_RX-	G61 G60	PCI Express Receive Input Differential Pairs 29	I PCIE		
PCIE30_TX+ PCIE30_TX-	H63 H62	PCI Express Transmit Output Differential Pairs 30	O PCIE		Not connected
PCIE30_RX+ PCIE30_RX-	G64 G63	PCI Express Receive Input Differential Pairs 30	I PCIE		
PCIE31_TX+ PCIE31_TX-	H66 H65	PCI Express Transmit Output Differential Pairs 31	O PCIE		Not connected
PCIE31_RX+ PCIE31_RX-	G67 G66	PCI Express Receive Input Differential Pairs 31	I PCIE		
PCIE32_TX+ PCIE32_TX-	E22 E21	PCI Express Transmit Output Differential Pairs 32	O PCIE		Not connected
PCIE32_RX+ PCIE32_RX-	F21 F20	PCI Express Receive Input Differential Pairs 32	I PCIE		
PCIE33_TX+ PCIE33_TX-	E25 E24	PCI Express Transmit Output Differential Pairs 33	O PCIE		Not connected
PCIE33_RX+ PCIE33_RX-	F24 F23	PCI Express Receive Input Differential Pairs 33	I PCIE		
PCIE34_TX+ PCIE34_TX-	E28 E27	PCI Express Transmit Output Differential Pairs 34	O PCIE		Not connected
PCIE34_RX+ PCIE34_RX-	F27 F26	PCI Express Receive Input Differential Pairs 34	I PCIE		
PCIE35_TX+ PCIE35_TX-	E31 E30	PCI Express Transmit Output Differential Pairs 35	O PCIE		Not connected
PCIE35_RX+ PCIE35_RX-	F30 F29	PCI Express Receive Input Differential Pairs 35	I PCIE		
PCIE36_TX+ PCIE36_TX-	E34 E33	PCI Express Transmit Output Differential Pairs 36	O PCIE		Not connected
PCIE36_RX+ PCIE36_RX-	F33 F32	PCI Express Receive Input Differential Pairs 36	I PCIE		
PCIE37_TX+ PCIE37_TX-	E37 E36	PCI Express Transmit Output Differential Pairs 37	O PCIE		Not connected
PCIE37_RX+ PCIE37_RX-	F36 F35	PCI Express Receive Input Differential Pairs 37	I PCIE		
PCIE38_TX+ PCIE38_TX-	E40 E39	PCI Express Transmit Output Differential Pairs 38	O PCIE		Not connected
PCIE38_RX+ PCIE38_RX-	F39 F38	PCI Express Receive Input Differential Pairs 38	I PCIE		

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PCIE39_TX+ PCIE39_TX-	E43 E42	PCI Express Transmit Output Differential Pairs 39	O PCIE		Not connected
PCIE39_RX+ PCIE39_RX-	F42 F41	PCI Express Receive Input Differential Pairs 39	I PCIE		
PCIE40_TX+ PCIE40_TX-	H21 H20	PCI Express Transmit Output Differential Pairs 40	O PCIE		Not connected
PCIE40_RX+ PCIE40_RX-	G22 G21	PCI Express Receive Input Differential Pairs 40	I PCIE		
PCIE41_TX+ PCIE41_TX-	H24 H23	PCI Express Transmit Output Differential Pairs 41	O PCIE		Not connected
PCIE41_RX+ PCIE41_RX-	G25 G24	PCI Express Receive Input Differential Pairs 41	I PCIE		
PCIE42_TX+ PCIE42_TX-	H27 H26	PCI Express Transmit Output Differential Pairs 42	O PCIE		Not connected
PCIE42_RX+ PCIE42_RX-	G28 G27	PCI Express Receive Input Differential Pairs 42	I PCIE		
PCIE43_TX+ PCIE43_TX-	H30 H29	PCI Express Transmit Output Differential Pairs 43	O PCIE		Not connected
PCIE43_RX+ PCIE43_RX-	G31 G30	PCI Express Receive Input Differential Pairs 43	I PCIE		
PCIE44_TX+ PCIE44_TX-	H33 H32	PCI Express Transmit Output Differential Pairs 44	O PCIE		Not connected
PCIE44_RX+ PCIE44_RX-	G34 G33	PCI Express Receive Input Differential Pairs 44	I PCIE		
PCIE45_TX+ PCIE45_TX-	H36 H35	PCI Express Transmit Output Differential Pairs 45	O PCIE		Not connected
PCIE45_RX+ PCIE45_RX-	G37 G36	PCI Express Receive Input Differential Pairs 45	I PCIE		
PCIE46_TX+ PCIE46_TX-	H39 H38	PCI Express Transmit Output Differential Pairs 46	O PCIE		Not connected
PCIE46_RX+ PCIE46_RX-	G40 G39	PCI Express Receive Input Differential Pairs 46	I PCIE		
PCIE47_TX+ PCIE47_TX-	H42 H41	PCI Express Transmit Output Differential Pairs 47	O PCIE		Not connected
PCIE47_RX+ PCIE47_RX-	G43 G42	PCI Express Receive Input Differential Pairs 47	I PCIE		
PCIE_BMC_TX+ PCIE_BMC_TX-	A60 A59	PCI Express Differential Transmit Pair for Carrier BMC	O PCIE		Not connected
PCIE_BMC_RX+ PCIE_BMC_RX-	B59 B58	PCI Express Differential Receive Pair for Carrier BMC	I PCIE		
PCIe_REFCLK0_LO+ PCIe_REFCLK0_LO-	C60 C59	Reference clock pair for PCIe lanes [0:7], also referred to as PCIe Group 0 Low and for the PCIe_BMC link	O LV_DIFF		
PCIe_REFCLK0_HI+ PCIe_REFCLK0_HI-	C57 C56	Reference clock pair for PCIe lanes [8:15] also referred to as PCIe Group 0 High	O LV_DIFF		

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PCIe_REFCLK1+ PCIe_REFCLK1-	E94 E93	Reference clock pair for PCIe lanes [16:31] also referred to as PCIe Group 1	O LV_DIFF		
PCIe_REFCLK2+ PCIe_REFCLK2-	F93 F92	Reference clock pair for PCIe lanes [32:47] also referred to as PCIe Group 2	O LV_DIFF		The PCIe lanes [32:47] are not connected.
PCIe_CLKREQ0_LO#	A56	PCIe reference clock request signal from Carrier devices for PCIe_REFCLK0_LO clock pair	Bi-Dir OD 3.3V	PU 10 KΩ 3.3 V	
PCIe_CLKREQ0_HI#	A57	PCIe reference clock request signal from Carrier devices for PCIe_REFCLK0_HI clock pair	Bi-Dir OD 3.3V	PU 10 KΩ 3.3 V	
PCIe_CLKREQ1#	E96	PCIe reference clock request signal from Carrier devices for PCIe_REFCLK1 clock pair	Bi-Dir OD 3.3V	PU 10 KΩ 3.3 V	
PCIe_CLKREQ2#	E97	PCIe reference clock request signals from Carrier devices for PCIe_REFCLK2 clock pair	Bi-Dir OD 3.3V	PU 10 KΩ 3.3 V	
PEG_LANE_REV#	G19	PCI Express Graphics lane reversal input strap. Pull low on the Carrier Board to reverse lane order, otherwise leave COM-HPC pin open. Pulled up on Module or Module chipset to chipset specific power rail.	I 3.3V	PU 100 KΩ 3.3 VSB	
PCI Express Additional Signals to Support Module-based PCIe Targets					
PCIe_REFCLKIN0+ PCIe_REFCLKIN0-	H93 H92	Reference clock inputs allowing Carrier based root to operate with Module based PCIe targets. The Module designer making use of these clocks should terminate them in a way appropriate to that design.	I LV_DIFF 3.3V		Not connected
PCIe_REFCLKIN1+ PCIe_REFCLKIN1-	H96 H95	Reference clock inputs allowing Carrier based root to operate with Module based PCIe targets. The Module designer making use of these clocks should terminate them in a way appropriate to that design.	I LV_DIFF 3.3V		Not connected
PCIe_WAKE_OUT0#	G100	Wake request signal from Module based PCIe Target to an off-Module PCIe Root complex.	OD 3.3VSB		Not connected
PCIe_WAKE_OUT1#	H100	Wake request signal from Module based PCIe Target to an off-Module PCIe Root complex.	OD 3.3VSB		Not connected
PCIe_PERST_IN0#	E100	Reset signals into Module to reset Module PCIe Targets.	I 3.3V	PD 100 KΩ	Not supported
PCIe_PERST_IN1#	F100	Reset signals into Module to reset Module PCIe Targets.	I 3.3V	PD 100 KΩ	Not supported

Note

The conga-HPC/cRLP cannot be used as a PCIe® target.

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Table 25 USB Signal Descriptions

USB	Pin #	Description	I/O	PU/PD	Comment
USB0+ USB0-	D17 D16	USB 2.0 differential pairs, channels 0 through 7. USB0 may be configured as a USB client or as a host, or both at the Module designer's discretion. All other USB ports, if implemented, shall be host ports. If any SuperSpeed ports are implemented, then they must be supported by a USB 2.0 port, using one of the USB[0:3] ports from this pool. Specific pairings are detailed below.	I/O USB 3.3 VSB		USB ports 0 and 1 require a PD controller and retimer to function with the default BIOS.
USB1+ USB1-	D14 D13		I/O USB 3.3 VSB		
USB2+ USB2-	C18 C17		I/O USB 3.3 VSB		
USB3+ USB3-	C15 C14		I/O USB 3.3 VSB		
USB4+ USB4-	B17 B16		I/O USB 3.3 VSB		
USB5+ USB5-	B14 B13		I/O USB 3.3 VSB		
USB6+ USB6-	A18 A17		I/O USB 3.3 VSB		
USB7+ USB7-	A15 A14		I/O USB 3.3 VSB		
USB0_SSTX0+ USB0_SSTX0-	D44 D43	Four sets of SuperSpeed differential pairs, used to realize one USB 3.2 Gen 2 2x2 port 0. Alternatively, USB 3.2 Gen 1 or Gen 2 ports (single TX pair, single RX pair per port) may be implemented using a portion of this interface. This port shall be used in conjunction with the corresponding USB 2.0 port pair (e.g. USB0 USB 2.0 differential pairs)	O USB SS		
USB0_SSRX0+ USB0_SSRX0-	C45 C44		I USB SS		
USB0_SSTX1+ USB0_SSTX1-	D47 D46		O USB SS		
USB0_SSRX1+ USB0_SSRX1-	C48 C47		I USB SS		
USB1_SSTX0+ USB1_SSTX0-	D38 D37	Four sets of SuperSpeed differential pairs, used to realize one USB 3.2 Gen 2 2x2 port 1. Alternatively, USB 3.2 Gen 1 or Gen 2 ports (single TX pair, single RX pair per port) may be implemented using a portion of this interface. This port shall be used in conjunction with the corresponding USB 2.0 port pair (e.g. USB1 USB 2.0 differential pairs)	O USB SS		
USB1_SSRX0+ USB1_SSRX0-	C39 C38		I USB SS		
USB1_SSTX1+ USB1_SSTX1-	D41 D40		O USB SS		
USB1_SSRX1+ USB1_SSRX1-	C42 C41		I USB SS		

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USB2_SSTX0+ USB2_SSTX0-	H03 H02	Four sets of SuperSpeed differential pairs, used to realize one USB 3.2 Gen 2 2x2 port 2. Alternatively, USB 3.2 Gen 1 or Gen 2 ports (single TX pair, single RX pair per port) may be implemented using a portion of this interface. This port shall be used in conjunction with the corresponding USB 2.0 port pair (e.g. USB2 USB 2.0 differential pairs)	O USB SS		
USB2_SSRX0+ USB2_SSRX0-	G04 G03		I USB SS		
USB2_SSTX1+ USB2_SSTX1-	H06 H05		O USB SS		
USB2_SSRX1+ USB2_SSRX1-	G07 G06		I USB SS		
USB3_SSTX0+ USB3_SSTX0-	H09 H08	Four sets of SuperSpeed differential pairs, used to realize one USB 3.2 Gen 2 2x2 port 3. Alternatively, USB 3.2 Gen 1 or Gen 2 ports (single TX pair, single RX pair per port) may be implemented using a portion of this interface. This port shall be used in conjunction with the corresponding USB 2.0 port pair (e.g. USB3 USB 2.0 differential pairs)	O USB SS		
USB3_SSRX0+ USB3_SSRX0-	G10 G09		I USB SS		
USB3_SSTX1+ USB3_SSTX1-	H12 H11		O USB SS		
USB3_SSRX1+ USB3_SSRX1-	G13 G12		I USB SS		
USB01_OC#	B28	USB over-current sense, USB channels 0,1; channels 2,3; channels 4,5 and channels 6,7 respectively. A pull-up for each of these lines to the 3.3V Suspend rail shall be present on the Module. The pull-up should be 10K. An open drain driver from USB current monitors on the Carrier Board may drive this line low. The Carrier Board shall not pull these lines up. Note that the over-current limits for USB 2.0 and USB 3.0 are different; this is a Carrier board implementation item.	I 3.3VSB	PU 10 KΩ 3.3 VSB	USB channels 0-3 share one over-current event.
USB23_OC#	B27			PU 10 KΩ 3.3 VSB	
USB45_OC#	B26			PU 10 KΩ 3.3 VSB	USB channels 4-7 share one over-current event.
USB67_OC#	B25			PU 10 KΩ 3.3 VSB	
RSMRST_OUT#	B86	USB devices that are to be powered in the S5 / S4 / S3 Suspend states should not have their 5V VBUS power enabled before RSMRST_OUT# transitions to the high state.	O 3.3 VSB	PD 100 KΩ	

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Table 26 USB4 Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB0_AUX+ USB0_AUX-	B44 B43	DisplayPort Aux channel for USB4® DP modes High speed differential pair	LV_DIFF		USB ports 0 and 1 require a PD controller and retimer to function with the default BIOS.
USB1_AUX+ USB1_AUX-	C36 C35	DisplayPort Aux channel for USB4® DP modes High speed differential pair	LV_DIFF		
USB2_AUX+ USB2_AUX-	H15 H14	DisplayPort Aux channel for USB4® DP modes High speed differential pair	LV_DIFF		Not connected
USB3_AUX+ USB3_AUX-	H18 H17	DisplayPort Aux channel for USB4® DP modes High speed differential pair	LV_DIFF		Not connected
USB0_LSTX	B41	Sideband TX interface for USB4® Alternate modes "Low Speed" asynchronous serial TX line	O 3.3 V	PD 1 MΩ	
USB0_LSRX	B40	Sideband RX interface for USB4® Alternate modes "Low Speed" asynchronous serial RX line	I 3.3 V	PD 1 MΩ	
USB1_LSTX	B39	Sideband TX interface for USB4 Alternate modes "Low Speed" asynchronous serial TX line	O 3.3 V	PD 1 MΩ	
USB1_LSRX	B38	Sideband RX interface for USB4® Alternate modes "Low Speed" asynchronous serial RX line	I 3.3 V	PD 1 MΩ	
USB2_LSTX	G18	Sideband TX interface for USB4® Alternate modes "Low Speed" asynchronous serial TX line	O 3.3 V	PD 1 MΩ	Not supported
USB2_LSRX	G17	Sideband RX interface for USB4® Alternate modes "Low Speed" asynchronous serial RX line	I 3.3 V	PD 1 MΩ	
USB3_LSTX	G16	Sideband TX interface for USB4® Alternate modes "Low Speed" asynchronous serial TX line	O 3.3 V	PD 1 MΩ	Not supported
USB3_LSRX	G15	Sideband RX interface for USB4® Alternate modes "Low Speed" asynchronous serial RX line	I 3.3 V	PD 1 MΩ	
SML0_DAT	B33	Data line for I2C data based System Management Links between chipset masters and Carrier. SML0 is used to control the Carrier based USB re-timers and	Bi-Dir OD 3.3 VSB	PU 499 RΩ 3.3 VSB	
SML1_DAT	B30	Data line for I2C data based System Management Links between chipset masters and Carrier. SML1 controls the Carrier based USB Power Delivery Controller.	Bi-Dir OD 3.3 VSB	PU 499 RΩ 3.3 VSB	
SML0_CLK	B32	Clock line for System Management Link 0. SML0 is used to support Carrier USB4® Re-Timers	Bi-Dir OD 3.3 V	PU 499 RΩ 3.3 VSB	
SML1_CLK	B29	Clock line for System Management Link 1. SML1 is used to support Carrier USB Power Delivery (PD) Controller.	Bi-Dir OD 3.3 V	PU 499 RΩ 3.3 VSB	
PMCALERT#	B31	Active low alert signal associated with the SML1 System Management link, from the Carrier based USB Power Delivery Controller.	I 3.3 V	PU 10 KΩ 3.3 VSB	

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USB_RT_ENA	B37	Power Enable for Carrier based USB Retimers. Sourced from chipset GPO. "USB Re-Timer Enable".	O 3.3 V	PD 10 KΩ	
USB_PD_I2C_DAT	B36	I2C data line between Module based Embedded Controller master and Carrier based USB Power Delivery Controller slave.	Bi-Dir OD 3.3 VSB	PU 1 KΩ 3.3 VSB	
USB_PD_I2C_CLK	B35	I2C clock line between Module based Embedded Controller master and Carrier based USB Power Delivery Controller slave.	Bi-Dir OD 3.3 VSB	PU 1 KΩ 3.3 VSB	
USB_PD_ALERT#	B34	Active low Alert signal from USB Power Delivery Controller to the Module Embedded Controller.	I 3.3 VSB	PU 100 KΩ 3.3 VSB	
Additional Signals to Support USB4® Implementation					
PLTRST#	A12	Platform Reset: output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low RSTBTN# input, a low VIN_PWR_OK input, a VCC power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software. PLTRST# should remain asserted (low) while the RSTBTN# is low.	O 3.3 VSB	PD 100 KΩ	
SUS_S4_S5#	C08	Indicates system is in Suspend to Disk (S4) or Soft Off (S5) state. Active low output.	O 3.3 VSB	PD 100 KΩ	

Table 27 eSPI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
eSPI_IO0 eSPI_IO1 eSPI_IO2 eSPI_IO3	A50 A51 A52 A53	eSPI Master Data Input / Outputs. These are bi-directional input/output pins used to transfer data between master and slaves.	I/O 1.8 VSB		
eSPI_CS0#	B54	eSPI Master Chip Select Outputs. A low selects a particular eSPI slave for the transaction. Each of the eSPI slaves is connected to a dedicated Chip Select pin. If an eSPI_CSx# pins is not in use, it shall be either pulled high or actively driven high.	O 1.8 VSB		
eSPI_CS1#	B55		O 1.8 VSB	PU 10 KΩ 1.8 VSB	Not supported
eSPI_CLK	A54	eSPI Master Clock Output. This pin provides the reference timing for all the serial input and output operations.	O 1.8 VSB		
eSPI_ALERT0#	B52	eSPI pins used by eSPI slave to request service from the eSPI master.	I 1.8 VSB	PU 10 KΩ 1.8 VSB	
eSPI_ALERT1#	B53		I 1.8 VSB	PU 10 KΩ 1.8 VSB	Not supported
eSPI_RST#	B56	eSPI Reset - resets the eSPI interface for both master and slaves. eSPI_RST# is typically driven from the eSPI master to eSPI slaves.	O 1.8 VSB	PD 75 KΩ	

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Table 28 Boot SPI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
BOOT_SPI_CS#	B48	Chip select for Carrier Board SPI If the BOOT_SPI_CS# pin is not in use, it shall be either pulled high or actively driven high.	O VCC_BOOT_SPI	PU 10 KΩ 3.3 VSB	
BOOT_SPI_IO0	C50	Bidirectional 4 bit data path out of and into a Carrier SPI flash operating in Serial Quad Interface (SQI) mode. If the flash memory device is operating in traditional Serial Peripheral Interface (SPI) mode, then signal BOOT_SPI_IO0 is used for getting serial data into the flash device (referred to as SI or MOSI in SPI Flash data sheets) and signal BOOT_SPI_IO1 is used to get serial data from the flash device (referred to as SO or MISO in flash data sheets)	I/O VCC_BOOT_SPI	PU 4.75 KΩ 3.3 VSB	
BOOT_SPI_IO1	C51				
BOOT_SPI_IO2 [1]	C52			PU 100 KΩ 3.3 VSB	
BOOT_SPI_IO3 [1]	C53			PU 100 KΩ 3.3 VSB	
BOOT_SPI_CLK	C54	Clock from Module chipset to Carrier SPI	O VCC_BOOT_SPI	PD 100K	
VCC_BOOT_SPI	B47	Power supply for Carrier Board SPI – sourced from Module – nominally 1.8 V or 3.3 V. The Module shall provide a minimum of 100 mA on VCC_BOOT_SPI. Carriers shall use less than 100 mA from this power source. VCC_BOOT_SPI shall only be used to power SPI devices on the Carrier Board. The Module vendor may choose what power domains the BOOT_SPI is active in.	Power (Out from Module)		3.3 VSB (active in suspend state)

Note

1. *This signal has a special functionality during the reset process. It may strap some basic important function of the module. For more information refer to section 9.2 "Boot Strap Signals".*

Table 29 BIOS Select Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
BSEL2	B51	Boot Select pins. These pins distinguish between an SPI or eSPI BIOS boot and between an on-Module or off-Module BIOS. Pulled up on Module to vendor specific power rail.	I 3.3 VSB	PU 10 KΩ 3.3 VSB	Pulled up to 3.3 VSB (active in suspend state)
BSEL1	B50		I 3.3 VSB	PU 10 KΩ 3.3 VSB	
BSEL0	B49		I 3.3 VSB	PU 10 KΩ 3.3 VSB	

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Table 30 DDI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
DDI0_PAIR0+ DDI0_PAIR0-	D23 D22	Digital Display Interface 0 differential pair 0	O LV_DIFF		
DDI0_PAIR1+ DDI0_PAIR1-	D26 D25	Digital Display Interface 0 differential pair 1	O LV_DIFF		
DDI0_PAIR2+ DDI0_PAIR2-	D29 D28	Digital Display Interface 0 differential pair 2	O LV_DIFF		
DDI0_PAIR3+ DDI0_PAIR3-	D32 D31	Digital Display Interface 0 differential pair 3	O LV_DIFF		
DDI1_PAIR0+ DDI1_PAIR0-	A24 A23	Digital Display Interface 1 differential pair 0	O LV_DIFF		
DDI1_PAIR1+ DDI1_PAIR1-	A27 A26	Digital Display Interface 1 differential pair 1	O LV_DIFF		
DDI1_PAIR2+ DDI1_PAIR2-	A30 A29	Digital Display Interface 1 differential pair 2	O LV_DIFF		
DDI1_PAIR3+ DDI1_PAIR3-	A33 A32	Digital Display Interface 1 differential pair 3	O LV_DIFF		
DDI2_PAIR0+ DDI2_PAIR0-	E07 E06	Digital Display Interface 2 differential pair 0	O LV_DIFF		
DDI2_PAIR1+ DDI2_PAIR1-	E10 E09	Digital Display Interface 2 differential pair 1	O LV_DIFF		
DDI2_PAIR2+ DDI2_PAIR2-	E13 E12	Digital Display Interface 2 differential pair 2	O LV_DIFF		
DDI2_PAIR3+ DDI2_PAIR3-	E16 E15	Digital Display Interface 2 differential pair 3	O LV_DIFF		
DDI0_DDC_AUX_SEL DDI1_DDC_AUX_SEL DDI2_DDC_AUX_SEL	C26 C28 E18	Selects the function of DDI[0:2]_SCL_AUX+ and DDI[0:2]_SDA_AUX-. If this input is unconnected on the Carrier, the AUX pair is used for the DP AUX+/- signals. If pulled or driven high on the Carrier, the AUX pair contains the TMDS[0:2] I2C CRTL_CLK and CTRL_DAT signals.	I 3.3 V	PD 1 MΩ	
DDI0_SCL_AUX+ DDI1_SCL_AUX+ DDI2_SCL_AUX+	D20 A21 E04	DP AUX+ function if DDI[0:2]_DDC_AUX_SEL is a no connect or driven to GND on the Carrier.	I/O LV_DIFF	PD 100 KΩ	
		TMDS I2C clock if DDI[0:2]_DDC_AUX_SEL is pulled or driven high on the Carrier.	I/O OD 3.3 V	PU 2.2 KΩ 3.3 V	
DDI0_SDA_AUX- DDI1_SDA_AUX- DDI2_SDA_AUX-	D19 A20 E03	DP AUX- function if DDI[0:2]_DDC_AUX_SEL is no connect.	I/O LV_DIFF	PU 100 KΩ 3.3 V	
		TMDS I2C data if DDI[0:2]_DDC_AUX_SEL is pulled high.	I/O OD 3.3 V	PU 2.2 KΩ 3.3 V	
DDI0_HPD DDI1_HPD DDI2_HPD	C28 C29 E19	DDI Hot-Plug Detect	I 3.3 V	PD 100 KΩ	

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Table 31 DisplayPort Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
DP0_LANE0+ DP0_LANE0-	D23 D22	Uni-directional main link for the transport of isochronous streams and secondary-data packets Multiplexed with DDI0_PAIR0+ and DDI0_PAIR0-	O LV_DIFF		
DP0_LANE1+ DP0_LANE1-	D26 D25	Uni-directional main link for the transport of isochronous streams and secondary-data packets Multiplexed with DDI0_PAIR1+ and DDI0_PAIR1-	O LV_DIFF		
DP0_LANE2+ DP0_LANE2-	D29 D28	Uni-directional main link for the transport of isochronous streams and secondary-data packets Multiplexed with DDI0_PAIR2+ and DDI0_PAIR2-	O LV_DIFF		
DP0_LANE3+ DP0_LANE3-	D32 D31	Uni-directional main link for the transport of isochronous streams and secondary-data packets Multiplexed with DDI0_PAIR3+ and DDI0_PAIR3-	O LV_DIFF		
DP1_LANE0+ DP1_LANE0-	A24 A23	Uni-directional main link for the transport of isochronous streams and secondary-data packets Multiplexed with DDI1_PAIR0+ and DDI1_PAIR0-	O LV_DIFF		
DP1_LANE1+ DP1_LANE1-	A27 A26	Uni-directional main link for the transport of isochronous streams and secondary-data packets Multiplexed with DDI1_PAIR1+ and DDI1_PAIR1-	O LV_DIFF		
DP1_LANE2+ DP1_LANE2-	A30 A29	Uni-directional main link for the transport of isochronous streams and secondary-data packets Multiplexed with DDI1_PAIR2+ and DDI1_PAIR2-	O LV_DIFF		
DP1_LANE3+ DP1_LANE3-	A33 A32	Uni-directional main link for the transport of isochronous streams and secondary-data packets Multiplexed with DDI1_PAIR3+ and DDI1_PAIR3-	O LV_DIFF		
DP2_LANE0+ DP2_LANE0-	E07 E06	Uni-directional main link for the transport of isochronous streams and secondary-data packets Multiplexed with DDI2_PAIR0+ and DDI2_PAIR0-	O LV_DIFF		
DP2_LANE1+ DP2_LANE1-	E10 E09	Uni-directional main link for the transport of isochronous streams and secondary-data packets Multiplexed with DDI2_PAIR1+ and DDI2_PAIR1-	O LV_DIFF		
DP2_LANE2+ DP2_LANE2-	E13 E12	Uni-directional main link for the transport of isochronous streams and secondary-data packets Multiplexed with DDI2_PAIR2+ and DDI2_PAIR2-	O LV_DIFF		
DP2_LANE3+ DP2_LANE3-	E16 E15	Uni-directional main link for the transport of isochronous streams and secondary-data packets Multiplexed with DDI2_PAIR3+ and DDI2_PAIR3-	O LV_DIFF		
DP0_AUX+ DP1_AUX+ DP2_AUX+	D20 A21 E04	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access Multiplexed with DDI[0:2]_SCL_AUX+	I/O LV_DIFF	PD 100 KΩ	

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DP0_AUX- DP1_AUX- DP2_AUX-	D19 A20 E03	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access Multiplexed with DDI[0:2]_SDA_AUX-	I/O LV_DIFF	PU 2.2 KΩ 3.3 V	
DP0_HPD DP1_HPD DP2_HPD	C28 C29 E19	Detection of Hot Plug / Unplug and notification of the link layer Multiplexed with DDI[0:2]_HPD	I 3.3 V	PD 100 KΩ	

Table 32 TMDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
TMDS0_CLK+ TMDS0_CLK-	D32 D31	TMDS0 Clock differential pair Multiplexed with DDI0_PAIR3+ and DDI0_PAIR3-	O LV_DIFF		
TMDS1_CLK+ TMDS1_CLK-	A33 A32	TMDS1 Clock differential pair Multiplexed with DDI1_PAIR3+ and DDI1_PAIR3-	O LV_DIFF		
TMDS2_CLK+ TMDS2_CLK-	E16 E15	TMDS3 Clock differential pair Multiplexed with DDI2_PAIR3+ and DDI2_PAIR3-	O LV_DIFF		
TMDS0_DATA0+ TMDS0_DATA0-	D29 D28	TMDS0 lane 0 differential pair Note that DDI and TMDS pair ordering is opposite Multiplexed with DDI0_PAIR2+ and DDI0_PAIR2-	O LV_DIFF		
TMDS0_DATA1+ TMDS0_DATA1-	D26 D25	TMDS0 lane 1 differential pair Note that DDI and TMDS pair ordering is opposite Multiplexed with DDI0_PAIR1+ and DDI0_PAIR1-	O LV_DIFF		
TMDS0_DATA2+ TMDS0_DATA2-	D23 D22	TMDS0 lane 2 differential pair Note that DDI and TMDS pair ordering is opposite Multiplexed with DDI0_PAIR2+ and DDI0_PAIR2-	O LV_DIFF		
TMDS1_DATA0+ TMDS1_DATA0-	A30 A29	TMDS1 lane 0 differential pair Note that DDI and TMDS pair ordering is opposite Multiplexed with DDI1_PAIR2+ and DDI1_PAIR2-	O LV_DIFF		
TMDS1_DATA1+ TMDS1_DATA1-	A27 A26	TMDS1 lane 1 differential pair Note that DDI and TMDS pair ordering is opposite Multiplexed with DDI1_PAIR1+ and DDI1_PAIR1-	O LV_DIFF		
TMDS1_DATA2+ TMDS1_DATA2-	A24 A23	TMDS1 lane 2 differential pair Note that DDI and TMDS pair ordering is opposite Multiplexed with DDI1_PAIR0+ and DDI1_PAIR0-	O LV_DIFF		
TMDS2_DATA0+ TMDS2_DATA0-	E13 E12	TMDS2 lane 0 differential pair Note that DDI and TMDS pair ordering is opposite Multiplexed with DDI2_PAIR2+ and DDI2_PAIR2-	O LV_DIFF		
TMDS2_DATA1+ TMDS2_DATA1-	E10 E09	TMDS2 lane 1 differential pair Note that DDI and TMDS pair ordering is opposite Multiplexed with DDI2_PAIR1+ and DDI2_PAIR1-	O LV_DIFF		

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TMDS2_DATA2+ TMDS2_DATA2-	E07 E06	TMDS2 lane 2 differential pair Note that DDI and TMDS pair ordering is opposite Multiplexed with DDI2_PAIR0+ and DDI2_PAIR0-	O LV_DIFF		
HDMI0_CTRL_CLK HDMI1_CTRL_CLK HDMI2_CTRL_CLK	D20 A21 E04	TMDS I2C control clock Multiplexed with DDI[0:2]_SCL_AUX+	I/O OD 3.3 V	PU 2.2 KΩ 3.3 V	
HDMI0_CTRL_DAT HDMI1_CTRL_DAT HDMI2_CTRL_DAT	D19 A20 E03	TMDS I2C control data Multiplexed with DDI[0:2]_SDA_AUX-	I/O OD 3.3 V	PU 2.2 KΩ 3.3 V	
HDMI0_HPD HDMI1_HPD HDMI2_HPD	C28 C29 E19	Detection of Hot Plug / Unplug and notification of the link layer Multiplexed with DDI[0:2]_HPD	I 3.3 V	PD 100 KΩ	

Table 33 eDP Embedded DisplayPort / MIPI DSI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
eDP_TX0+ eDP_TX0-	A39 A38	eDP / DSI differential data pairs Multiplexed with DSI_TX1+ and DSI_TX1-	O LV_DIFF		MIPI DSI is not supported
eDP_TX1+ eDP_TX1-	A42 A41	eDP / DSI differential data pairs Multiplexed with DSI_TX2+ and DSI_TX2-	O LV_DIFF		MIPI DSI is not supported
eDP_TX2+ eDP_TX2-	A45 A44	eDP differential data pair DSI differential clock pair Multiplexed with DSI_CLK+ and DSI_CLK-	O LV_DIFF		MIPI DSI is not supported
eDP_TX3+ eDP_TX3-	A48 A47	eDP / DSI differential data pairs Multiplexed with DSI_TX3+ and DSI_TX3-	O LV_DIFF		MIPI DSI is not supported
eDP_AUX+ eDP_AUX-	A36 A35	eDP AUX channel differential pair DSI differential data pair Multiplexed with DSI_TX0+ and DSI_TX0-	I/O LV_DIFF		MIPI DSI is not supported
eDP_VDD_EN	C31	eDP / DSI power enable Multiplexed with DSI_VDD_EN	O 3.3 V	PD 100 KΩ	MIPI DSI is not supported
eDP_BKLT_EN	C32	eDP / DSI backlight enable Multiplexed with DSI_BKLT_EN	O 3.3 V	PD 100 KΩ	MIPI DSI is not supported
eDP_BKLT_CTRL	C33	EDP / DSI backlight brightness control Multiplexed with DSI_BKLT_CTRL	O 3.3 V		MIPI DSI is not supported
eDP_HPD	C30	eDP: Detection of Hot Plug / Unplug and notification of the link layer Multiplexed with DSI_TE DSI: Tearing Effect Input: this is an optional signal from the DSI display (that has it's own display controller and frame buffer) coordinating with the host display controller.	I 3.3 V	PD 100 KΩ	MIPI DSI is not supported

Note

MIPI DSI is not supported.

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Table 34 CSI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
CSI0_RX0+ CSI0_RX0-	G73 G72	CSI0 differential data input pairs 0	I LV_DIFF		Not supported
CSI0_RX1+ CSI0_RX1-	G76 G75	CSI0 differential data input pairs 1	I LV_DIFF		Not supported
CSI0_RX2+ CSI0_RX2-	G79 G78	CSI0 differential data input pairs 2	I LV_DIFF		Not supported
CSI0_RX3+ CSI0_RX3-	G82 G81	CSI0 differential data input pairs 3	I LV_DIFF		Not supported
CSI1_RX0+ CSI1_RX0-	H72 H71	CSI1 differential data input pairs 0	I LV_DIFF		Not supported
CSI1_RX1+ CSI1_RX1-	H75 H74	CSI1 differential data input pairs 1	I LV_DIFF		Not supported
CSI1_RX2+ CSI1_RX2-	H78 H77	CSI1 differential data input pairs 2	I LV_DIFF		Not supported
CSI1_RX3+ CSI1_RX3-	H81 H80	CSI1 differential data input pairs 3	I LV_DIFF		Not supported
CSI0_CLK+ CSI0_CLK-	G85 G84	CSI0 differential clock input pairs	I LV_DIFF		Not supported
CSI1_CLK+ CSI1_CLK-	H84 H83	CSI1 differential clock input pairs	I LV_DIFF		Not supported
CSI0_MCLK CSI1_MCLK	G89 H88	CSI Master Clock outputs for CSI0 and CSI1	O 1.8V		Not supported
CSI0_I2C_DAT	G88	CSI-2 Mode: I2C Data line	I/O OD 1.8 V	PU 1.5 KΩ 1.8 V	Not supported
CSI1_I2C_DAT	H87	CSI-2 Mode: I2C Data line	I/O OD 1.8 V	PU 1.5 KΩ 1.8 V	Not supported
CSI0_I2C_CLK	G87	CSI-2 Mode: I2C Clock line	O OD 1.8 V	PU 1.5 KΩ 1.8 V	Not supported
CSI1_I2C_CLK	H86	CSI-2 Mode: I2C Clock line	O OD 1.8 V	PU 1.5 KΩ 1.8 V	Not supported
CSI0_RST#	G90	Active low Reset signals for CSI port 0	O 1.8 V		Not supported
CSI1_RST#	H89	Active low Reset signals for CSI port1	O 1.8 V		Not supported
CSI0_ENA	G91	Active high Enable signals for CSI port 0	O 1.8 V		Not supported
CSI1_ENA	H90	Active high Enable signals for CSI port 1	O 1.8 V		Not supported

Note

MIPI CSI-2® requires driver support from the silicon vendor. The driver was not available at the time of writing. Contact congatec support for more information.

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Table 35 Soundwire Audio Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SNDW_DMIC_DAT0	C24	Bi-directional PCM audio data	I/O 1.8 V		Not supported
SNDW_DMIC_DAT1	C21	Bi-directional PCM audio data	I/O 1.8 V		Not supported
SNDW_DMIC_CLK0	C23	Clock for Soundwire transactions	O 1.8 V		Not supported
SNDW_DMIC_CLK1	C20	Clock for Soundwire transactions	O 1.8 V		Not supported

Table 36 I2S / Soundwire / HDA Audio Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
I2S_CLK/ SNDW_CLK2/ HDA_BITCLK	B23	I2S Clock Alternative use as Soundwire 2 clock or Serial data clock generated by the external HDA codec	O 1.8 V		I2S and SNDW are not supported
I2S_DIN/ SNDW_DAT2/ HDA_SDIN	B22	I2S Data In. This pin is an input in I2S mode. Alternative use as bi-directional Soundwire 2 data lane or Serial TDM data input	I/O 1.8 V		I2S and SNDW are not supported
I2S_DOUT/ SNDW_DAT3/ HDA_SDOUT [1]	B20	I2S Data Out. This pin is an input in I2S mode Alternative use as bi-directional Soundwire 2 data lane or Serial TDM data output to the codec	I/O 1.8 V	For HDA_SDOUT: PD 100 KΩ	I2S and SNDW are not supported
I2S_LRCLK/ SNDW_CLK3/ HDA_SYNC	B19	I2S L/R Clock Alternative use as Soundwire 3 clock or Sample-synchronization signal to the codec	O 1.8 V		I2S and SNDW are not supported
I2S_MCLK/ HDA_RST#	B21	I2S Master Clock Alternative use as Reset output to codec; active low	O 1.8 V		I2S is not supported

Note

1. *This signal has a special functionality during the reset process. It may strap some basic important function of the module. For more information refer to section 9.2 "Boot Strap Signals".*

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Table 37 Asynchronous Serial Port Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
UART0_TX	C89	Logic level asynchronous serial port transmit signal	O 3.3 V		
UART0_RX	C90	Logic level asynchronous serial port receive signal	I 3.3 V	PU 47.5 KΩ 3.3 V	
UART0_RTS#	C91	Logic level asynchronous serial port Request to Send signal, active low	O 3.3 V		
UART0_CTS#	C92	Logic level asynchronous serial port Clear to Send input, active low	I 3.3 V	PU 47.5 KΩ 3.3 V	
UART1_TX	B87	Logic level asynchronous serial port transmit signal	O 3.3 V		
UART1_RX	B88	Logic level asynchronous serial port receive signal	I 3.3 V	PU 47.5 KΩ 3.3 V	
UART1_RTS#	B89	Logic level asynchronous serial port Request to Send signal, active low	O 3.3 V		
UART1_CTS#	B90	Logic level asynchronous serial port Clear to Send input, active low	I 3.3 V	PU 47.5 KΩ 3.3 V	

Table 38 I2C Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
I2C0_CLK	C93	Clock I/O line for the general purpose I2C0 port	I/O OD 3.3 VSB	PU 4.75 KΩ 3.3 VSB	
I2C0_DAT	C94	Data I/O line for the general purpose I2C0 port	I/O OD 3.3 VSB	PU 4.75 KΩ 3.3 VSB	
I2C0_ALERT#	C95	Alert input / interrupt for I2C0	I 3.3 VSB	PU 4.75 KΩ 3.3 VSB	
I2C1_CLK [1]	C96	Clock I/O line for the general purpose I2C1 port	I/O OD 1.8 VSB	PU 4.75 KΩ 1.8 VSB	Not supported
I2C1_DAT [1]	C97	Data I/O line for the general purpose I2C1 port	I/O OD 1.8 VSB	PU 4.75 KΩ 1.8 VSB	Not supported

Note

1. *The conga-HPC/cRLP does not support I2C1.*

Table 39 IPMB Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
IPMB_CLK	B91	Clock I/O line for the multi-master IPMB port	I/O OD 3.3 VSB	PU 4.75 KΩ 3.3 VSB	
IPMB_DAT	B92	Data I/O line for the multi-master IPMB port	I/O OD 3.3 VSB	PU 4.75 KΩ 3.3 VSB	

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Table 40 General Purpose SPI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GP_SPI_MISO	B94	Serial data into the COM-HPC Module from the Carrier GP_SPI device ("Master In Slave Out")	I 3.3 V	PU 10 KΩ 3.3 V	
GP_SPI_MOSI	B93	Serial data from the COM-HPC Module to the Carrier GP_SPI device ("Master Out Slave In")	O 3.3 V		
GP_SPI_CLK	B99	Clock from the Module to Carrier GP_SPI device	O 3.3 V		
GP_SPI_CS0#	B95	GP_SPI chip selects, active low	O 3.3 V	PU 10 KΩ 3.3 V	
GP_SPI_CS1#	B96			PU 10 KΩ 3.3 V	
GP_SPI_CS2#	B97			PU 10 KΩ 3.3 V	Not supported
GP_SPI_CS3#	B98			PU 10 KΩ 3.3 V	Not supported
GP_SPI_ALERT#	B100	Alert (interrupt) from a Carrier GP_SPI device to the Module	I 3.3 V	PU 10 KΩ 3.3 V	

Table 41 Power and System Management Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PWRBTN#	B02	A falling edge creates a power button event. Power button events can be used to bring a system out of S5 soft off and other suspend states, as well as powering the system down (with a sustained low).	I 3.3 VSB	PU 100 KΩ 3.3 VSB	
RSTBTN#	C02	Reset button input. The RSTBTN# may be level sensitive (active low) or may be triggered by the falling edge of the signal. The Module PLTRST# signal (below) should not be released (driven or pulled high) while the RSTBTN# is low. For situations when RSTBTN# is not able to reestablish control of the system, VIN_PWR_OK or a power cycle may be used.	I 3.3 VSB	PU 10 KΩ 3.3 VSB	
PLTRST#	A12	Platform Reset: output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low RSTBTN# input, a low VIN_PWR_OK input, a VCC power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software. PLTRST# should remain asserted (low) while the RSTBTN# is low.	O 3.3 VSB	PD 100 KΩ	
VIN_PWR_OK	C06	Power OK from main power supply. A high value indicates that the power is good.	I 3.3 VSB	PU 100 KΩ 3.3 VSB	

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SUS_S3#	B08	Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_S3# on the Carrier Board should be used to enable the non-standby power on a typical ATX supply. Even in single input supply system implementations (AT mode, no standby input), the SUS_S3# Module output should be used to disable any Carrier voltage regulators when SUS_S3# is low, to prevent bleed leakage from Carrier circuits into the Module.	O 3.3 VSB	PD 100 KΩ	
SUS_S4_S5#	C08	Indicates system is in Suspend to Disk (S4) or Soft Off (S5) state. Active low output.	O 3.3 VSB	PD 100 KΩ	
SUS_CLK	A87	32.768 kHz +/- 100 ppm clock used by Carrier peripherals such as M.2 cards in their low power modes.	O 3.3 VSB		
WAKE0#	D10	PCI Express wake up signal.	I/O 3.3 VSB	PU 1 KΩ 3.3 VSB	
WAKE1#	D11	General purpose wake up signal. May be used to implement wake- up on PS2 keyboard or mouse activity.	I 3.3 VSB	PU 10 KΩ 3.3 VSB	
BATLOW#	A11	Indicates that external battery is low. This port provides a battery-low signal to the Module for orderly transitioning to power saving or power cut-off ACPI modes.	I 3.3 VSB	PU 10 KΩ 3.3 VSB	
LID#	B45	LID switch. Low active signal used by the ACPI operating system for a LID switch.	I 3.3 VSB	PU 10 KΩ 3.3 VSB	
SLEEP#	B46	Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.	I 3.3 VSB	PU 100 KΩ 3.3 VSB	
TAMPER#	B06	Tamper or Intrusion detection line on VCC_RTC power well. Carrier hardware pulls this low on a Tamper event.	I 3.3 VSB	PU 1 MΩ 3.3 VSB	
AC_PRESENT	D34	Driven hard low on Carrier if system AC power is not present	I 3.3 VSB	PU 100 KΩ 3.3 VSB	
RSMRST_OUT#	B86	This is a buffered copy of the internal Module RSMRST# (Resume Reset, active low) signal. The internal Module RSMRST# signal is an input to the chipset or SOC and when it transitions from low to high it indicates that the suspend well power rails are stable. USB devices on the Carrier that are to be active in S5 / S3 / S0 should not have their 5V supply applied before RSMRST_OUT# goes high. RSMRST_ OUT# shall be a 3.3V CMOS Module output, active in all power states.	O 3.3 VSB	PD 100 KΩ	

Table 42 Rapid Shutdown Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
RAPID_SHUTDOWN	E01	Trigger for Rapid Shutdown. Must be driven to 5 V though a <= 50 Ω source impedance for ≥ 20 µs. Pull-down / disable on Module if RAPID_SHUTDOWN pin is not asserted.	I 5 VSB	PD 100 KΩ	Not supported

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Table 43 Thermal Protection Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
CARRIER_HOT#	C04	Input from off-Module temp sensor indicating an over-temp situation.	I 3.3 V	PU 10 KΩ 3.3 V	
THERMTRIP#	B04	Active low output indicating that the CPU has entered thermal shutdown.	O 3.3 V	PD 100 KΩ	

Table 44 SMBus Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SMB_CLK	C86	System Management Bus bidirectional clock line.	I/O OD 3.3 VSB	PU 2.2 KΩ 3.3 VSB	
SMB_DAT	C87	System Management Bus bidirectional data line.	I/O OD 3.3 VSB	PU 2.2 KΩ 3.3 VSB	
SMB_ALERT#	C88	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.	I 3.3 VSB	PU 2.2 KΩ 3.3 VSB	

Table 45 General Purpose Input Output Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GPIO_00	A88	General purpose input / output pins. Upon a hardware reset, these pins should be configured as inputs. As inputs, these pins should be able to generate an interrupt to the Module host.	I/O 3.3 VSB	PU 100 KΩ 3.3 VSB	
GPIO_01	A89				
GPIO_02	A90				
GPIO_03	A91				
GPIO_04	A92				
GPIO_05	A93				
GPIO_06	A94				
GPIO_07	A95				
GPIO_08	A96				
GPIO_09	A97				
GPIO_10	A98				
GPIO_11	A99				

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Table 46 Module Type Definition Signal Description

<table>
<tr><th>Signal</th><th>Pin #</th><th>Description</th><th>I/O</th><th>Comment</th></tr>
<tr><td>TYPE0
TYPE1
TYPE2</td><td>A100
C100
D100</td><td>The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the Module. The pins are tied on the Module to either ground (GND) or are no-connects (NC). These pins shall be pulled up on the Carrier, to Carrier standby voltage rail of 5 V or less. Carrier hardware reads the level on these straps.
<table>
<tr><th></th><th colspan="3">Module Connections</th><th rowspan="2">Meaning</th></tr>
<tr><th>Ref</th><th>TYPE2</th><th>TYPE1</th><th>TYPE0</th></tr>
<tr><td>7</td><td>NC</td><td>NC</td><td>NC</td><td>Reserved</td></tr>
<tr><td>6</td><td>NC</td><td>NC</td><td>GND</td><td>Reserved</td></tr>
<tr><td>5</td><td>NC</td><td>GND</td><td>NC</td><td>Reserved</td></tr>
<tr><td>4</td><td>NC</td><td>GND</td><td>GND</td><td>Server module - Fixed 12 V input</td></tr>
<tr><td>3</td><td>GND</td><td>NC</td><td>NC</td><td>Reserved</td></tr>
<tr><td>2</td><td>GND</td><td>NC</td><td>GND</td><td>Reserved</td></tr>
<tr><td>1</td><td>GND</td><td>GND</td><td>NC</td><td>Client module - Wide range 8 V to 20 V input</td></tr>
<tr><td>0</td><td>GND</td><td>GND</td><td>GND</td><td>Client module - Fixed 12 V input</td></tr>
</table>
The module shall implement all three TYPE[x] pins per the table above.
The carrier board should implement combinatorial logic that monitors the Module TYPE pins and keeps power off (e.g deactivates the ATX PS_ON# signal to an ATX power supply or otherwise deactivates VCC to the COM- HPC Module) if an incompatible Module pin-out type is detected. All three TYPE[x] pins should be monitored by the Carrier. The Carrier Board logic may also implement a fault indicator such as an LED.</td><td>PDS</td><td>The conga-HPC/cRLP is a Ref 1 Type module (Client module - Wide range 8 V to 20 V input). Therefore, the TYPE2, TYPE1 are connected to GND and TYPE0 is NC.</td></tr>
</table>

Table 47 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
WD_OUT	B11	Output indicating that a watchdog time-out event has occurred. Refer to the COM-HPC® Module Base Specification for details.	O 3.3 V	PD 100 KΩ	
WD_STROBE#	B10	Strobe input to watchdog timer. Periodic strobing prevents the watchdog, if enabled, from timing out.	I 3.3 V	PU 10 KΩ 3.3 V	
FAN_PWMOUT	C11	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	O OD 3.3 V		
FAN_TACHIN	C12	Fan tachometer input for a fan with a two pulse output.	I OD 3.3 V	PU 47.5 KΩ 3.3 V	
TEST#	B85	Module input to allow vendor specific Module test mode(s). Carrier designers should leave this pin open on the Carrier. Designers involved in the design of specialty Carriers for Module test may pull this line to GND or possibly to a Module specific analog voltage between GND and 3.3 V to select a test mode.	I OD 3.3 VSB	PU 10 KΩ 3.3 VSB	Do not connect on carrier board

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RSVD	D35	Reserved pins. These may be assigned functions in future versions of this specification. Reserved pins shall not be connected to anything, and shall not be connected to each other.			Not connected
	E69-E77				
	E84-E85				
	F12-F18				
	F68-F69				
	F83-F84				
	F95				
	G69-G70				
	G93-G94				
	H68-H69				

Table 48 External Power Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC	A01-A09	Primary power input: fixed +12 V on the Client Type 0; wide range +8 V to +20 V on the Client Type 1; fixed +12 V on the Server. All available VCC pins on the connector shall be used. Refer to COM-HPC® Module Base Specification for details.			
	B01, B03, B05, B07, B09				
	C01, C03, C05, C07, C09				
	D01-D09				
VCC_5V_SBY	B24	Standby power input: +5.0 V nominal. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design. Refer to COM-HPC® Module Base Specification for details.			
	G01				
VCC_RTC	A86	Real-time clock circuit-power input. Nominally +3.0 V. Refer to COM-HPC® Module Base Specification for details.			

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Table 49 Functional Safety (FuSa) Support Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
FUSA_STATUS0	F01	Two bit FuSa staus / error indication outputs to Carrier based Safety Controller hardware 00 - power off 01 - no error (OK state) 10 - error state (NOK state) 11 - reset state	O CMOS 3.3 V		Not connected
FUSA_STATUS1	F02		O CMOS 3.3 V		Not connected
FUSA_ALERT#	F03	Active low output from the COM-HPC Module that signals the occurrence of a correctable error on the COM-HPC Module; the carrier FuSa Safety Controller should query the status via the FuSa SPI interface	O CMOS 3.3 V		Not connected
FUSA_SPI_CS#	F04	Active low chip select into the COM-HPC Module from the Carrier FuSa Safety Controller SPI Master	I CMOS 3.3 V	PU 10 KΩ 3.3 V	Not supported
FUSA_SPI_CLK	F05	Clock into the COM-HPC Module from the Carrier FuSa Safety Controller SPI Master	I CMOS 3.3 V	PU 10 KΩ 3.3 V	Not supported
FUSA_SPI_MISO	F06	Serial data into the Carrier FuSa SPI Master from the COM-HPC Module SPI Slave (“Master In Slave Out”)	O CMOS 3.3 V		Not connected
FUSA_SPI_MOSI	F07	Serial data from the Carrier FuSa SPI Master, into the COM-HPC Module SPI Slave (“Master Out Slave In”)	I CMOS 3.3 V	PU 10 KΩ 3.3 V	Not supported
FUSA_SPI_ALERT	F08	Active high alert output from the COM-HPC Module to alert the Carrier FuSa Safety Controller that Module FuSa SPI data is available for transfer	O CMOS 3.3 V		Not connected
FUSA_VOLTAGE_ERR#	F09	Active low output indicating an over- or under voltage or over-current condition of the monitored voltage rails of the FuSa relevant module power supply	O CMOS 3.3 V		Not connected
PROCHOT#	F10	Active low output indicating a temperature excursion event on the COM-HPC Module	O CMOS 3.3 V	PD 100KΩ	
CATERR#	F11	Active low output indicating a catastrophic error on the COM-HPC CPU or SOC	O CMOS 3.3 V	PD 100KΩ	
THERMTRIP#	B04	Active low output indicating that the CPU has entered thermal shutdown	O CMOS 3.3 V	PD 100KΩ	

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9.2 Boot Strap Signals

Table 50 Boot Strap Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
I2S_DOUT/ SNDW_DAT3/ HDA_SDOUT	B20	I2S Data Out. This pin is an input in I2S mode Alternative use as bi-directional Soundwire 2 data lane or Serial TDM data output to the codec	I/O 1.8 V	For HDA_SDOUT: PD 100 KΩ	I2S and SNDW are not supported
BOOT_SPI_IO2	C52	Bidirectional 4 bit data path out of and into a Carrier SPI flash operating in Serial Quad Interface (SQI) mode.	I/O VCC_BOOT_SPI	PU 100 KΩ 3.3 VSB	
BOOT_SPI_IO3	C53	Bidirectional 4 bit data path out of and into a Carrier SPI flash operating in Serial Quad Interface (SQI) mode.	I/O VCC_BOOT_SPI	PU 100 KΩ 3.3 VSB	

Note

The signals listed in the table above are used as chipset configuration straps during system reset. In this condition (during reset), the COM-HPC® or chipset internally implemented resistors pull these signals to the correct state.

Caution

No external DC loads or external pull-up or pull-down resistors should change the configuration of the signals listed in the above table. External resistors may override the internal strap states and cause the COM-HPC® module to malfunction and/or cause irreparable damage to the module.

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10 System Resources

10.1 I/O Address Assignment

The I/O address assignment of the conga-HPC/cRLP module is functionally identical with a standard PC/AT.

The BIOS assigns PCI and PCI Express I/O resources from FFF0h downwards. Non PnP/PCI/PCI Express compliant devices must not consume I/O resources in that area.

10.2 PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00h	00h	00h	Bridge Device - Host/PCI bridge
00h	02h	00h	Display Controller - VGA/8514 controller
00h	06h	00h	Bridge Device - PCI/PCI bridge
00h	06h	02h	Bridge Device - PCI/PCI bridge
00h	07h	00h	Bridge Device - PCI/PCI bridge
00h	07h	01h	Bridge Device - PCI/PCI bridge
00h	0Dh	00h	Serial Bus Controllers – USB
00h	0Dh	02h	Serial Bus Controllers – USB
00h	14h	00h	Serial Bus Controllers – USB
00h	14h	02h	Memory Controller - RAM memory controller – Shared SRAM
00h	15h	00h	Serial Bus Controllers - Other bus type
00h (only H-series CPU)	16h	00h	Simple Communications Controllers - Other communication – Intel Management Interface (Intel MEI)
00h	17h	00h	Mass Storage Controller – SATA Interface
00h	1Ch	00h	PCI Express Root Port 1
00h	1Ch	03h	PCI Express Root Port 4
00h	1Ch	04h	PCI Express Root Port 5
00h	1Dh	00h	PCI Express Root Port 9
00h	1Dh	01h	PCI Express Root Port 10
00h	1Fh	00h	Bridge Device - PCI/ISA bridge - Enhanced SPI Interface
00h	1Fh	03h	Multimedia Device – High-Definition Audio Interface
00h	1Fh	04h	Serial Bus Controllers - System Management Bus
00h	1Fh	05h	Serial Bus Controllers – Other bus type
57h	00h	00h	Network Controller - Ethernet controller – i225LM/V/IT
58h	00h	00h	Network Controller - Ethernet controller – i225LM/V/IT

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Note

1. *In the standard configuration, the Intel Management Engine (ME) related devices are partly present or not present at all.*
2. *The PCI Express Ports are visible only if a device is attached to the PCI Express Slot on the carrier board.*
3. *The Table represents a case when a Single function PCI/PCIe device is connected to all possible slots on the carrier board. The given bus numbers will change based on actual hardware configuration.*
4. *Internal PCI devices not connected to the conga-HPC/cRLP are not listed.*

10.3 I²C

The addresses below are reserved for Battery Management solutions. Onboard resources are not connected to the I²C busses.

Table 51 Reserved I2C Bus Addresses

8-bit Device Address	7-bit Device Address	Device	Description
0x14	0x0A	congatec Board Controller	Reserved for battery management
0x16	0x0B	congatec Board Controller	Reserved for battery management

10.4 SMBus

The addresses below are reserved on the SMBus of the conga-HPC/cRLP. The SMBus signals are connected to the Intel® chipset.

Table 52 Reserved SMBus Addresses

8-bit Device Address	7-bit Device Address	Device	Comment
0xA0	0x50	Memory SPD	Reserved only if SM BUS isolation is not set to "Always" Check further devices on DDR5 memory.
0xA4	0x52		
0x14	0x0A	congatec Board Controller	Reserved for battery management
0x16	0x0B	congatec Board Controller	Reserved for battery management

Note

Do not use the SMBus for off-board non-system management devices. For more information, contact congatec technical support.

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10.5 USB PD Bus

The addresses below are reserved on the USB Power Delivery Bus (USB PD Bus) of the conga-HPC/cRLP.

Table 53 Reserved USB PD Bus Addresses

8-bit Device Address	7-bit Device Address	Device	Description
0x40	0x20	Carrier board Post Code Display	Reserved for carrier board Post Code Display
0x42	0x21		

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11 BIOS Setup Description

The BIOS setup description of the conga-HPC/cRLP can be viewed without having access to the module. However, access to the restricted area of the congatec website is required in order to download the necessary tool (CgMlfViewer) and Menu Layout File (MLF).

The MLF contains the BIOS setup description of a particular BIOS revision. The MLF can be viewed with the CgMlfViewer tool. This tool offers a search function to quickly check for supported BIOS features. It also shows where each feature can be found in the BIOS setup menu.

For more information, read the application note "AN42 - BIOS Setup Description" available at www.congatec.com.

Note

If you do not have access to the restricted area of the congatec website, contact your local congatec sales representative.

11.1 Navigating the BIOS Setup Menu

The BIOS setup menu shows the features and options supported in the congatec BIOS. To access and navigate the BIOS setup menu, press the <DEL> or <F2> key during POST. The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

11.2 BIOS Versions

The BIOS displays the BIOS project name and the revision code during POST, and on the main setup screen. The initial production BIOS for conga-HPC/cRLP is identified as GxAPR1xx, where:

- R is the identifier for a BIOS ROM file,
- 1 is the so called feature number and
- xx is the major and minor revision number.

The binary size is 32 MB.

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11.3 Updating the BIOS

BIOS updates are recommeded to correct platform issues or enhance the feature set of the module. The conga-HPC/cRLP features a congatec/AMI AptioEFI firmware on an onboard flash ROM chip. You can update the firmware with the congatec System Utility. The utility has five versions—UEFI shell, DOS based command line[1], Win32 command line, Win32 GUI, and Linux version.

For more information about "Updating the BIOS" refer to the user's guide for the congatec System Utility "CGUTLm1x.pdf" on the congatec website at www.congatec.com.

Note

1. *Deprecated*

Caution

The DOS command line tool is not officially supported by congatec and therefore not recommended for critical tasks such as firmware updates. We recommend to use only the UEFI shell for critical updates.

11.3.1 Update from External Flash

For instructions on how to update the BIOS from external flash, refer to the AN7_External_BIOS_Update.pdf application note on the congatec website at www.congatec.com.

11.4 Supported Flash Devices

The conga-HPC/cRLP supports the following flash devices:

- Winbond W25R256JVEIQ 32 MB
- Macronix MX25L25645G 32 MB

The flash devices can be used on the carrier board to support external BIOS. For more information about external BIOS support, refer to the Application Note "AN7_External_BIOS_Update.pdf" on the congatec website at www.congatec.com.

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