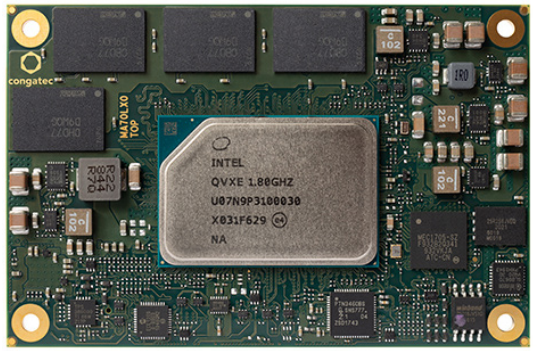

conga-MA7

COM Express® 3.0 Type 10 Mini Module with Intel® Elkhart Lake Processors

User's Guide

Revision 1.03

Revision History

Revision	Date (yyyy-mm-dd)	Author	Changes
0.1	2021-08-20	BEU	• Preliminary release
1.00	2023-01-09	BEU	• Added note to section 2.2 "Supported Operating Systems" and updated section 6.3.4 "OEM BIOS Code/Data" because CSM is no longer supported • Added power consumption values to table 7 "Power Consumption Values" and 8 " CMOS Battery Power Consumption" • Added note about missing non-legacy UART drivers to section 5.8 "UART/CAN" • Added inrush and current values to section 5.13 "Power Control" • Added information to section 9 "System Resources" • Added supported flash device to section 10.4 "Supported Flash Devices"
1.01	2023-07-27	BEU	• Renamed section 1.1 "conga-MA7 Options Information" to "Options Information" • Added CPU use conditions, Tjunction, and DTR information to Table 2 and 3 • Added note about a Windows 10 issue with S3 to section 2.2 "Supported Operating Systems" • Updated section 6.2.3 "Power Loss Control" • Updated section 6.2.5 "Enhanced Soft-Off State" • Renamed section 9.4 "SM Bus" to "SMBus"
1.02	2024-01-15	BEU	• Updated title page • Updated RoHS Directive in preface section • Added note to section 2.7 "Environmental Specifications" • Added note to section 4 "Cooling Solutions" • Added note to sections 5.7 "SD Card" • Added note to sections 6.1.1 "eMMC" • Updated section 6.2.3 "Power Loss Control"
1.03	2024-11-11	BEU	• Added reference to additional documents to preface section • Updated supported OS in section 2.1 "Feature List" and 2.2 "Supported Operating Systems" • Updated humidity range in section 2.1 "Feature List" and 2.7 "Environmental Specifications" • Added section 6.1 "Integrated Real-Time Hypervisor" • Added note regarding watchdog NMI mode support to section 6.3.4 "Watchdog"

Preface

This user's guide provides information about the components, features, connectors and BIOS Setup menus available on the conga-MA7. It is one of three documents that should be referred to when designing a COM Express® application. The other reference documents that should be used include the following:

COM Express® Design Guide
COM Express® Specification

The links to the COM Express® documents can be found on the PICMG® website at www.picmg.org

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Warning

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Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.

Note

Notes call attention to important information that should be observed.

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Terminology

Term	Description
GB	Gigabyte
GHz	Gigahertz
kB	Kilobyte
MB	Megabyte
Mbit	Megabit
kHz	Kilohertz
MHz	Megahertz
TDP	Thermal Design Power
PCIe	PCI Express
SATA	Serial ATA
DDC	Display Data Channel
SoC	System On Chip
LVDS	Low-Voltage Differential Signaling
GbE	Gigabit Ethernet
MLC	Multi-level Cell
SLC	Single-level Cell
HDA	High Definition Audio
cBC	congatec Board Controller
I/F	Interface
N.C.	Not connected
N.A.	Not available
TBD	To be determined

Contents

List of Tables

1 Introduction

COM Express® is an open industry standard defined specifically for COMs (Computer-on-Modules). Its creation makes it possible to smoothly transition from legacy interfaces to the newest technologies available today. COM Express® modules are available in following form factors:

- Mini 84 mm x 55 mm
- Compact 95 mm x 95 mm
- Basic 125 mm x 95 mm
- Extended 155 mm x 110 mm

The COM Express® Specification Rev 3.0 currently defines three different pinout types. These are shown in the table below.

Table 1 COM Express 3.0 Pinout Types

Types	Connector Rows	PCIe Lanes	PEG	SATA Ports	LAN ports	USB 2.0 / SuperSpeed USB	Display Interfaces
Type 6	A-B C-D	Up to 24	1	Up to 4	1	Up to 8 / 4 [1]	VGA,LVDS/eDP, PEG, 3x DDI
Type 7	A-B C-D	Up to 32	-	Up to 2	5 (1x 1 Gb, 4x 10 Gb)	Up to 4 / 4 [1]	
Type 10	A-B	Up to 4	-	Up to 2	1	Up to 8 / 2 [1]	LVDS/eDP, 1xDDI

1. *The SuperSpeed USB ports are not in addition to the USB 2.0 ports.*

The conga-MA7 modules use the Type 10 pinout definition and comply with the COM Express® 3.0 specification. They are equipped with single 220-pin high performance connector that ensure stable data throughput.

The COM integrates all the core components of a common PC and is mounted onto an application-specific carrier board. COM modules are legacy-free design (no Super I/O, PS/2 keyboard and mouse) and provide most of the functional requirements for any application. These functions include, but are not limited to a rich complement of contemporary high bandwidth serial interfaces such as PCI Express, Serial ATA, USB 2.0, and Gigabit Ethernet. The robust thermal and mechanical concept, combined with extended power-management capabilities, is perfectly suited for all applications.

Carrier board designers can use as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration.

Most importantly, COM Express® modules are scalable. Once an application has been created, the product range can be diversified by using different performance-class or form-factor size modules. Simply unplug one module and replace it with another; redesign is not necessary.

1.1 Options Information

The conga-MA7 is available in eight variants (five commercial and three industrial). The tables below show the different configurations available.

Table 2 Commercial Variants

Part-No.		049400	049401	049402	049420	049421
Processor		Intel® Atom® x6425E 2.0 GHz, Quad Core	Intel® Atom® x6413E 1.5 GHz, Quad Core	Intel® Atom® x6211E 1.3 GHz, Dual Core	Intel® Pentium® J6426 2.0 GHz, Quad Core	Intel® Celeron® J6413 1.8 GHz, Quad Core
Burst Freq.		3.0 GHz	3.0 GHz	3.0 GHz	3.0 GHz	3.0 GHz
Graphics Engine		Intel® UHD Graphics	Intel® UHD Graphics	Intel® UHD Graphics	Intel® UHD Graphics	Intel® UHD Graphics
GFX Base/Burst Freq.		500 / 750 MHz	500 / 750 MHz	350 / 750 MHz	400 / 850 MHz	400 / 800 MHz
Onboard Memory (LPDDR4x)		16 GB, 3200 MT/s quad channel	8 GB, 3200 MT/s quad channel	8 GB, 3200 MT/s quad channel	16 GB, 3200 MT/s quad channel	8 GB, 3733 MT/s quad channel
eMMC		64 GB	32 GB	32 GB	64 GB	32 GB
Processor TDP (Max)		12 W	9 W	6 W	10 W	10 W
CPU Use Condition [1, 2]		Embedded	Embedded	Embedded	PC Client	PC Client
CPU Tjunction	Min.	-40°C	-40°C	-40°C	0°C	0°C
	Max.	105°C	105°C	105°C	105°C	105°C
DTR (Cold to Hot Transition) [3]		T_{Boot} + 90°C	T_{Boot} + 90°C	T_{Boot} + 90°C	T_{Boot} + 70°C	T_{Boot} + 70°C
DTR (Hot to Cold Transition) [3]		T_{Boot} - 90°C	T_{Boot} - 90°C	T_{Boot} - 90°C	T_{Boot} - 70°C	T_{Boot} - 70°C

Table 3 Industrial Variants

Part-No.		049410	049411	049412
Processor		Intel® Atom® x6425RE 1.9 GHz, Quad Core	Intel® Atom® x6414RE 1.5 GHz, Quad Core	Intel® Atom® x6212RE 1.2 GHz, Dual Core
Burst Freq.		N.A	N.A	N.A
Graphics Engine		Intel® UHD Graphics	Intel® HD Graphics 500	Intel® HD Graphics 505
GFX Base/Burst Freq.		400 MHz / N.A	400 MHz / N.A	350 MHz / N.A
Onboard Memory (LPDDR4x)		8 GB, 4266 MT/s quad channel	4 GB, 3200 MT/s quad channel	4 GB, 3200 MT/s quad channel
eMMC		32 GB	32 GB	32 GB
Processor TDP (Max)		12 W	9 W	6 W
CPU Use Condition [1, 2]		Industrial	Industrial	Industrial
CPU Tjunction	Min.	-40°C	-40°C	-40°C
	Max.	110°C	110°C	110°C
DTR (Cold to Hot Transition) [3, 4]		T_{Boot} + 90°C T_{Boot} + 110°C	T_{Boot} + 90°C T_{Boot} + 110°C	T_{Boot} + 90°C T_{Boot} + 110°C
DTR (Hot to Cold Transition) [3, 4]		T_{Boot} - 90°C T_{Boot} - 110°C	T_{Boot} - 90°C T_{Boot} - 110°C	T_{Boot} - 90°C T_{Boot} - 110°C

Note

1. *Intel SoC use conditions. For more information, see Intel documentation.*
2. *Disable Turbo mode for industrial use conditions.*
3. *T_{Boot} is the boot temperature. If the Tjunction is not within the DTR range, you must reboot the system. See Intel documentation for more information.*
4. *For DTR of ±110°C, the speed of any enabled USB 3.1 port must be limited to 5 Gb/s.*

2 Specifications

2.1 Feature List

Table 4 Feature Summary

Form Factor	COM Express® Mini; Type 10	
Processor	Intel® Atom®, Pentium® and Celeron® SoCs	
DRAM	Max. 16 GB onboard LPDDR4x; up to 4.267 MT/s	
Ethernet	Intel® GbE with TSN support; real-time trigger	
I/O Interfaces	4x PCIe Gen3 2x USB 3.1 Gen2 6x USB 2.0 2x SATA III up to 2x UART up to 1x CAN	GPIO I²C Bus SMBus SPI LPC 1x SDIO (option)
Mass Storage	eMMC 5.1 onboard flash up to 64GB (option for 256 GB)	
Audio	Intel® HD Audio	
Graphics	Intel® UHD Graphics (Gen11)	
LVDS	Single channel LVDS interface up to 1280x1024@60Hz; shared with eDP up to 4096x2160@60Hz (option)	
Digital Display Interface	DisplayPort 1.4 4096x2160@60Hz	
congatec Board Controller	Multistage watchdog; non volatile user data storage; manufacturing and board Information; board statistics; fast mode and multi master I²C bus; power loss control	
Embedded BIOS Feature	AMI Aptio® UEFI firmware; 32 MByte serial SPI with congatec Embedded BIOS features; OEM Logo; OEM CMOS Defaults; LCD Control; Display Auto Detection; Backlight Control; Flash Update	
Power Management	ACPI 5 .0 compliant; Smart Battery Management	
Operating Systems	Microsoft® Windows 11; Microsoft® Windows 11 IoT Enterprise; Microsoft® Windows 10; Microsoft® Windows 10 IoT Enterprise; Linux; Yocto	
Hypervisor	RTS Real-Time Hypervisor	
Temperature Range	Commercial variants: Industrial variants:	Operating Temperature: 0 to +60°C Operating Temperature: -40 to +85°C
		Storage Temperature: -20 to +80°C Storage Temperature: -40 to +85°C
Relative Humidity	Operating: Storage:	10 to 85% r. H. non cond. 5 to 85% r. H. non cond.
Size	84 x 55 mm	

2.2 Supported Operating Systems

The conga-MA7 supports the following operating systems:

- Microsoft® Windows® 11, 64-bit (version 22H2 and later)
- Microsoft® Windows® 11 IoT Enterprise, 64-bit (version 22H2 and later)
- Microsoft® Windows® 10, 64-bit (version 22H2 and later)
- Microsoft® Windows® 10 IoT Enterprise, 64-bit (version 22H2 and later)
- Linux Ubuntu (64-bit)
- Yocto (64-bit)
- RTS Hypervisor

Note

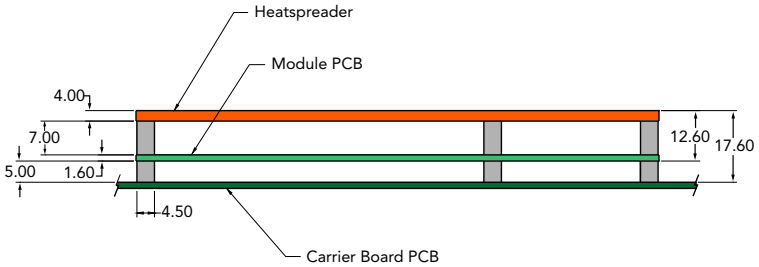
1. *Windows® 10 version 21H2 (OS build 19044) may sporadically fail to wake from S3 sleep state (POST Code: 0300). congatec recommends updating to a later Windows® 10 version.*

2. *For the installation of Windows® 10, congatec recommends a minimum storage capacity of 20 GB. congatec will not offer technical support for systems with less than 20 GB storage space.*

3. *The conga-MA7 only supports native UEFI operating systems. Legacy operating systems that require the Compatibility Support Module (CSM) as part of the UEFI firmware are not supported.*

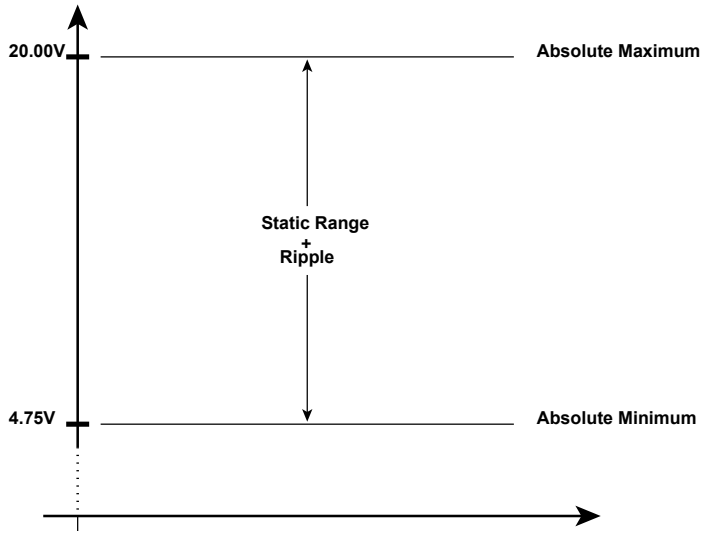
2.3 Mechanical Dimensions

- 84.0mm x 55.0mm
- Height approximately 18 or 21mm (including heatspreader) depending on the carrier board connector that is used. If the 5mm (height) carrier board connector is used then approximate overall height is 18mm. If the 8mm (height) carrier board connector is used then approximate overall height is 21mm



2.4 Supply Voltage Standard Power

- 4.75V - 20V (Wide input range)



2.4.1 Electrical Characteristics

Power supply pins on the module's connectors limit the amount of input power. The following table provides an overview of the limitations for pinout Type 10 (single connector, 220 pins).

Table 5 Power Limits on Type 10 Connector

Power Rail	Module Pin Current Capability (A)	Nominal Input (V)	Input Range (V)	Derated Input (V)	Max. Input Ripple (10Hz to 20MHz) (mV)	Max. Module Input Power (w. derated input) (W)	Assumed Conversion Efficiency	Max. Load Power (W)
VCC_12V	6	12	11.4 - 12.6	11.4	+/- 100	68	85%	58
Wide Input	6		4.75-20.0	4.75	+/- 100	28		
VCC_5V_SBY	2	5	4.75-5.25	4.75	+/- 50	9		
VCC_RTC	0.5	3	2.0-3.3		+/- 20			

2.4.2 Rise Time

The input voltages shall rise from 10% of nominal to 95% of nominal within 0.1 ms to 20 ms (0.1 ms ≤ Rise Time ≤ 20 ms). Each DC input voltage must rise from 10% to 90% of its nominal voltage in a smooth, continuous ramp and the slope of the turn-on waveform must be positive.

2.5 Power Consumption

The power consumption values were measured with the following setup:

- Input voltage +5 V
- conga-MA7 COM
- modified congatec carrier board
- conga-MA7 cooling solution
- Microsoft Windows® 10 (64-bit)

Note

The CPU was stressed to its maximum workload with the Intel® Thermal Analysis Tool.

The power consumption values were recorded during the following system states:

Table 6 Measurement Description

System State	Description	Comment
S0: Minimum value	Lowest frequency mode (LFM) with minimum core voltage during desktop idle.	
S0: Maximum value	Highest frequency mode (HFM/Turbo Boost).	The CPU was stressed to its maximum frequency.
S0: Peak value	Highest power spike during the measurement of "S0: Maximum value". This state shows the peak value over a short period of time (worst case power consumption value).	Consider this value when designing the system's power supply to ensure that sufficient power is supplied during worst case scenarios.
S3	COM is powered by VCC_5V, while in Suspend to RAM state	
S5	COM is powered by VCC_5V, while in Soft-Off state	
S5e	COM is powered by VCC_5V, while in enhanced Soft-Off state	

Note

The peripherals did not influence the measured values because they were powered externally.

The tables below provide additional information about the power consumption data for each of the conga-MA7 variants offered. The values are recorded at various operating modes.

Table 7 Power Consumption Values

Part-No.	Memory Size	H.W Rev.	BIOS Rev.	CPU			Current (A) @ 12V (S0) or 5V (S3, S5, S5e)					
				Variant	Cores	Base / Burst Freq. (GHz)	S0: Min	S0: Max	S0: Peak	S3	S5	S5e
049400	16 GB	B.4	TBD	Intel® Atom® x6425E	4	2.0 / 3.0	0.32	1.59	2.20	0.30	0.30	0.03
049401	8 GB	B.4	TBD	Intel® Atom® x6413E	4	1.5 / 3.0	0.32	1.46	2.12	0.29	0.28	0.03
049402	8 GB	B.4	TBD	Intel® Atom® x6211E	2	1.3 / 3.0	0.32	0.94	1.76	0.35	0.30	0.03
049410	8 GB	B.4	TBD	Intel® Atom® x6425RE	4	1.9 / N.A	0.33	1.24	1.41	0.30	0.30	0.03
049411	4 GB	B.4	TBD	Intel® Atom® x6414RE	4	1.5 / N.A	0.32	0.94	1.09	0.29	0.31	0.03
049412	4 GB	B.4	TBD	Intel® Atom® x6212RE	2	1.2 / N.A	0.32	0.71	0.87	0.29	0.29	0.03
049420	16 GB	B.4	TBD	Intel® Pentium® J6426	4	2.0 / 3.0	0.28	1.36	2.15	0.31	0.30	0.03
049421	8 GB	B.4	TBD	Intel® Celeron® J6413	4	1.8 / 3.0	0.25	1.32	2.06	0.30	0.29	0.03

Note

With fast input voltage rise time, the inrush current may exceed the measured peak current.

2.6 Supply Voltage Battery Power

Table 8 CMOS Battery Power Consumption

RTC @	Voltage	Current
-10°C	3V DC	5.42 µA
20°C	3V DC	5.96 µA
70°C	3V DC	8.4 µA

Note

1. *Do not use the CMOS battery power consumption values listed above to calculate CMOS battery lifetime.*
2. *Measure the CMOS battery power consumption in your customer specific application in worst case conditions (for example, during high temperature and high battery voltage).*
3. *Consider also the self-discharge of the battery when calculating the lifetime of the CMOS battery. For more information, refer to application note "AN09 RTC Battery Lifetime" at www.congatec.com.*
4. *We recommend to always have a CMOS battery present when operating the conga-MA7.*

2.7 Environmental Specifications

Temperature (commercial variants)	Operation:	0° to 60°C	Storage: -20° to +80°C
Temperature (industrial variants)	Operation:	-40° to 85°C	Storage: -40° to +85°C
Humidity	Operation:	10% to 85%	Storage: 5% to 85%

Caution

The above operating temperatures must be strictly adhered to at all times. When using a congatec heatspreader, the maximum operating temperature refers to any measurable spot on the heatspreader's surface.

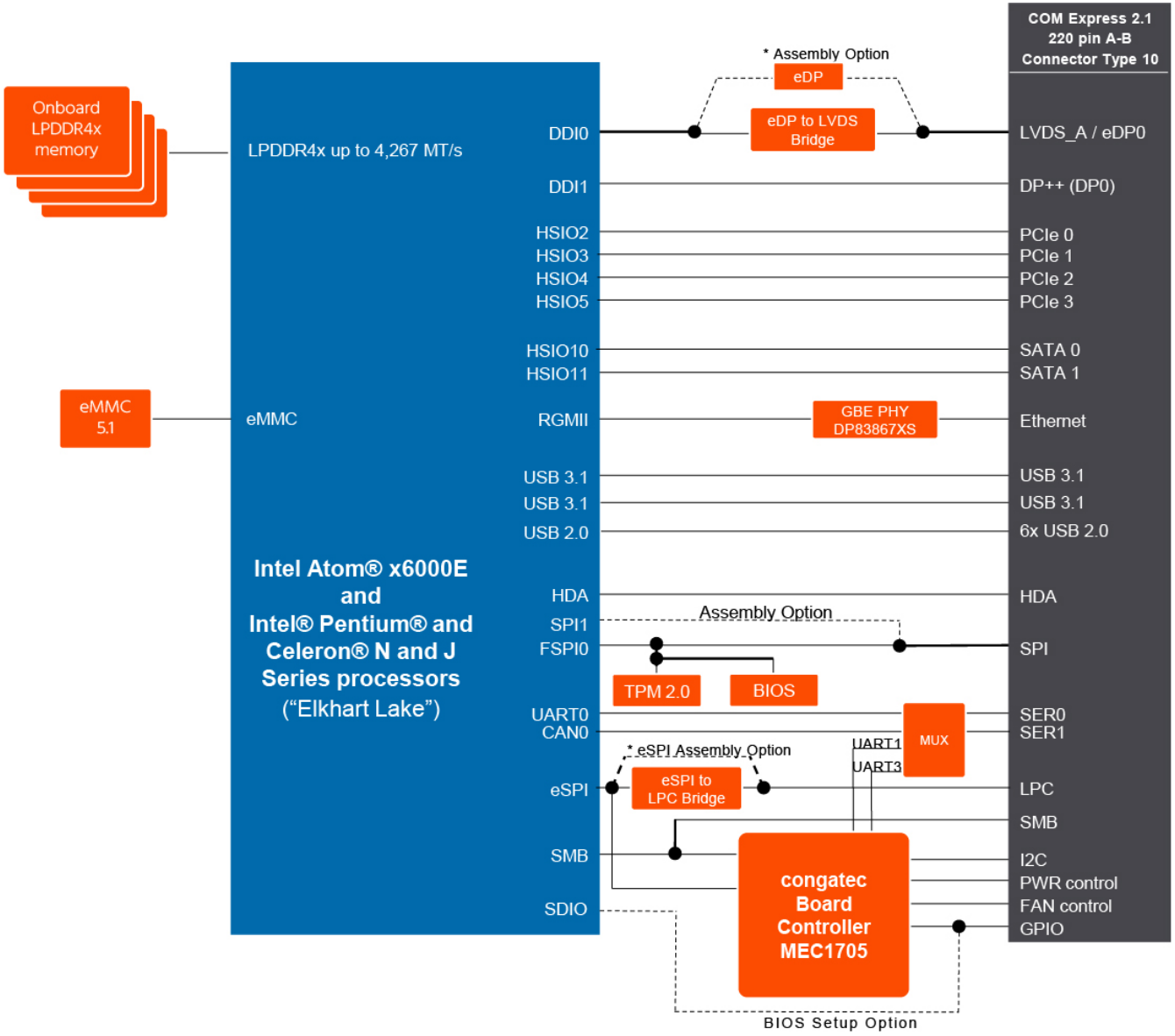
Humidity specifications are for non-condensing conditions.

Note

For long term storage of the conga-MA7 (more than six months), keep the conga-MA7 in a climate-controlled building at a constant temperature between 5°C and 40°C, with humidity of less than 65% and at an altitude of less than 3000 m. Also ensure the storage location is dry and well ventilated.

We do not recommend storing the conga-MA7 for more than five years under these conditions.

3 Block Diagram



Note: * Assembly options on request only

4 Cooling Solutions

congatec GmbH offers the following cooling solutions for the conga-MA7 variants. The dimensions of the cooling solutions are shown in the sub-sections. All measurements are in millimeters.

Table 9 Cooling Solution Variants

Cooling Solution	Part-No.	Description
HSP	049454	Heatspreader for conga-MA7 with lidded Intel Atom x6000E processors. All standoffs are with 2.7mm bore hole.
	049455	Heatspreader for conga-MA7 with lidded Intel Atom x6000E processors. All standoffs are M2.5mm threaded.
	049456	Heatspreader for conga-MA7 with bare-die Intel Pentium/Celeron N and J processors. All standoffs are with 2.7mm bore hole.
	049457	Heatspreader for conga-MA7 with bare-die Intel Pentium/Celeron N and J processors. All standoffs are M2.5mm threaded.
CSP	049450	Passive cooling solution for conga-MA7 with lidded Intel Atom x6000E processors. All standoffs are with 2.7mm bore hole.
	049451	Passive cooling solution for conga-MA7 with lidded Intel Atom x6000E processors. All standoffs are M2.5mm threaded.
	049452	Passive cooling solution for conga-MA7with bare-die Intel Pentium/Celeron N and J processors. All standoffs are with 2.7mm bore hole.
	049453	Passive cooling solution for conga-MA7 with bare-die Intel Pentium/Celeron N and J processors. All standoffs are M2.5mm threaded.

Caution

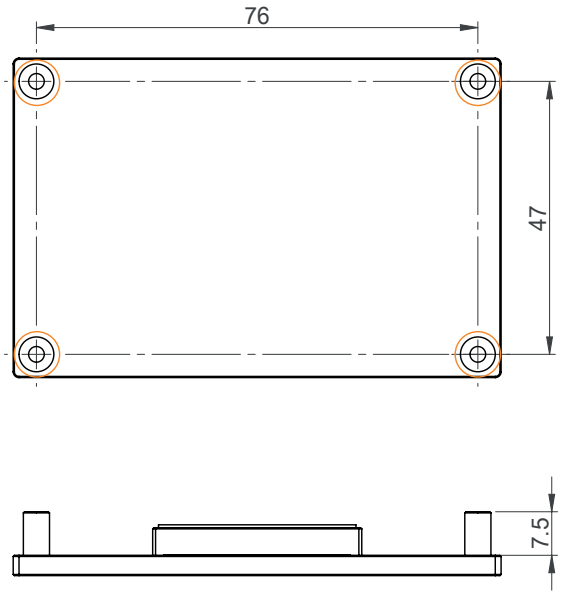
1. *The congatec heatspreaders/cooling solutions are tested only within the commercial temperature range of 0° to 60°C. Therefore, if your application that features a congatec heatspreader/cooling solution operates outside this temperature range, ensure the correct operating temperature of the module is maintained at all times. This may require additional cooling components for your final application's thermal solution.*
2. *For adequate heat dissipation, use the mounting holes on the cooling solution to attach it to the module. Apply thread-locking fluid on the screws if the cooling solution is used in a high shock and/or vibration environment. To prevent the standoff from stripping or cross-threading, use non-threaded carrier board standoffs to mount threaded cooling solutions.*
3. *For applications that require vertically-mounted cooling solution, use only coolers that secure the thermal stacks with fixing post. Without the fixing post feature, the thermal stacks may move.*
4. *Do not exceed the recommended maximum torque. Doing so may damage the module or the carrier board, or both.*

Note

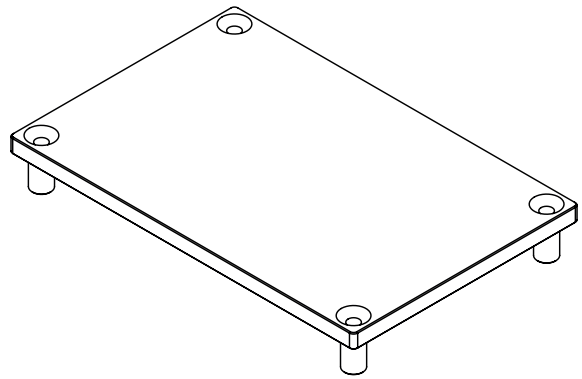
1. *We recommend a maximum torque of 0.4 Nm for carrier board mounting screws.*
2. *The gap pad material used on congatec heatspreaders may contain silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.*
3. *For optimal thermal dissipation, do not store the congatec cooling solutions for more than six months.*

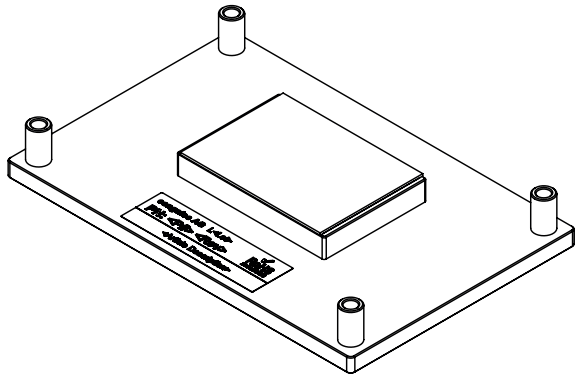
4.1 HSP Dimensions

Lidded Variants (Part-No.: 049454, 049455)

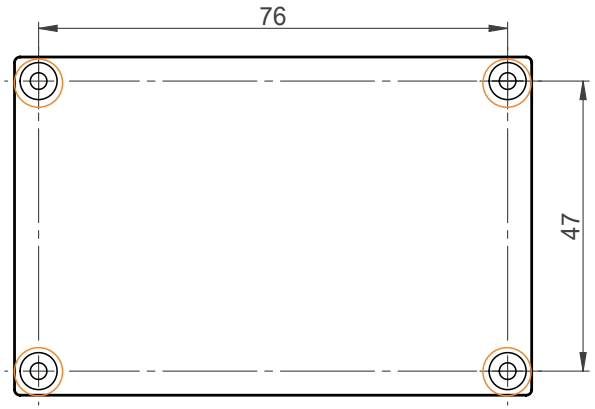


M2.5 x 6 mm threaded standoff for threaded version
or
ø2.7 x 6 mm non-threaded standoff for borehole version

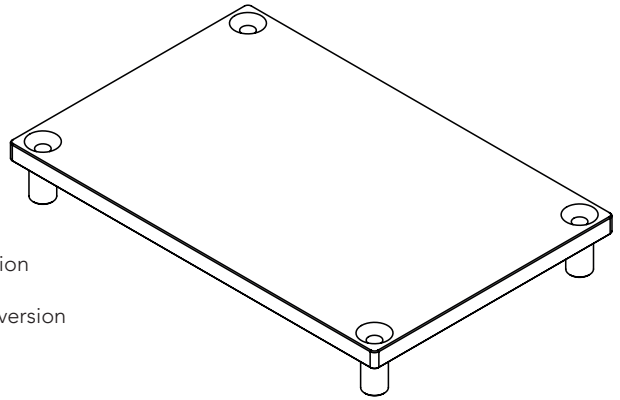


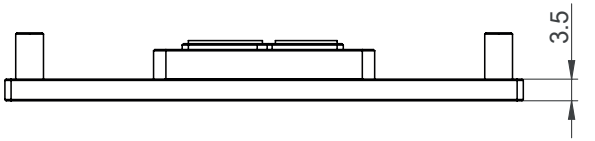


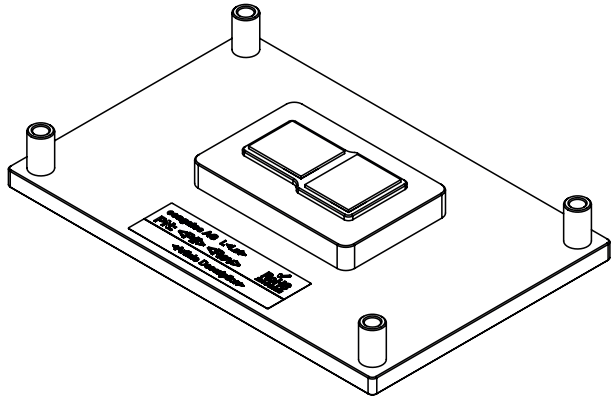
Bare-Die Variants (Part-No.: 049456, 049457)

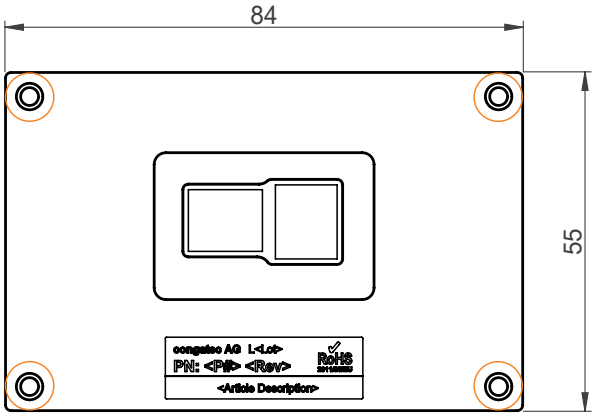


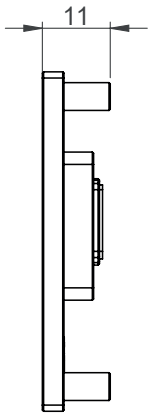
M2.5 x 6 mm threaded standoff for threaded version
or
ø2.7 x 6 mm non-threaded standoff for borehole version





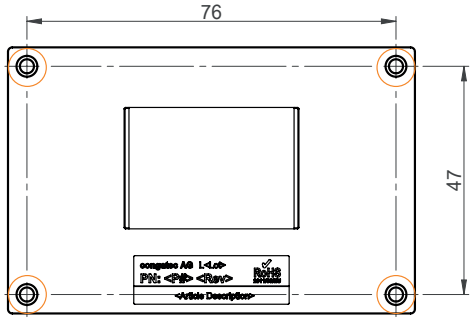




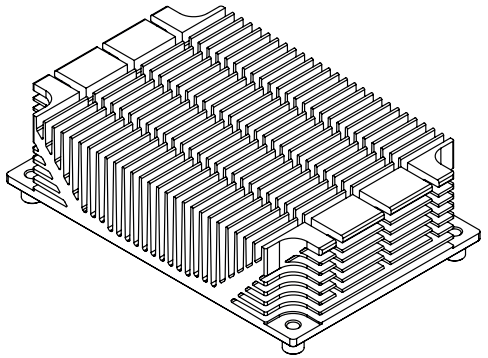


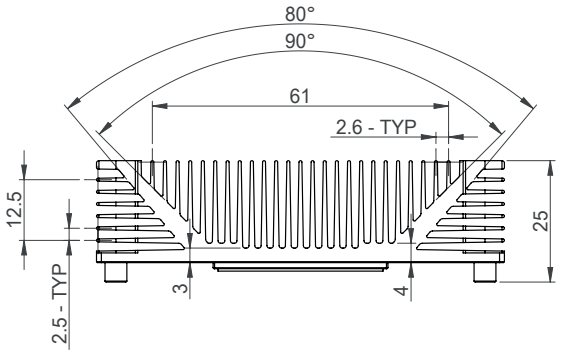
4.2 CSP Dimensions

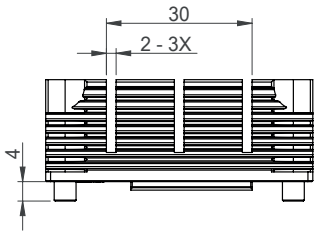
Lidded Variants (Part-No.: 049450, 049451)

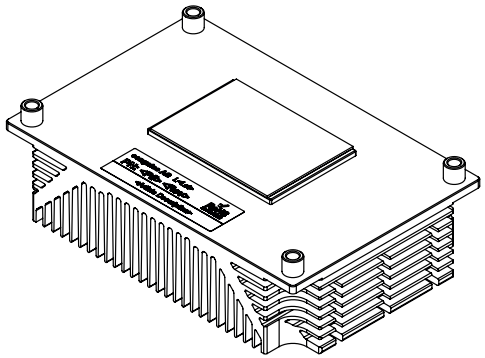


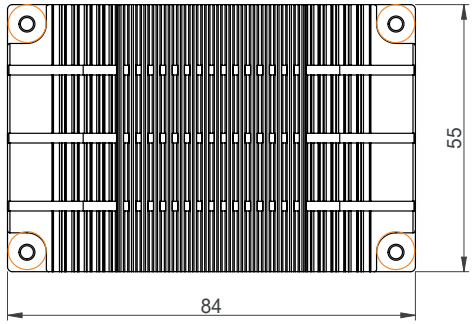
M2.5 x 6 mm threaded standoff for threaded version
or
ø2.7 x 6 mm non-threaded standoff for borehole version



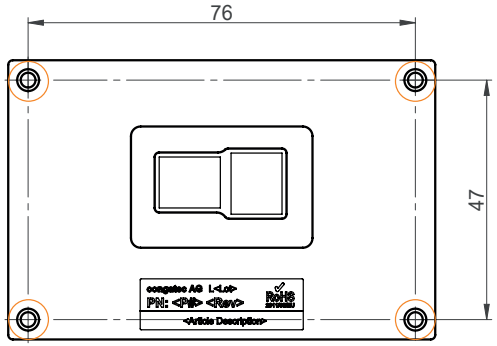




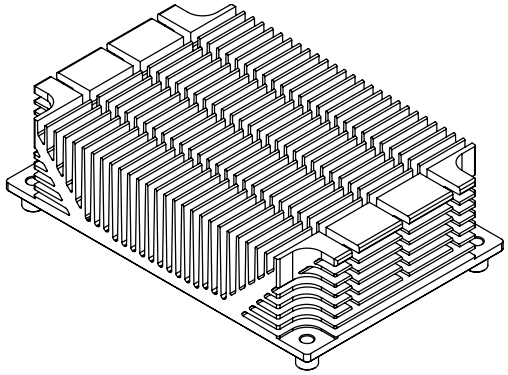


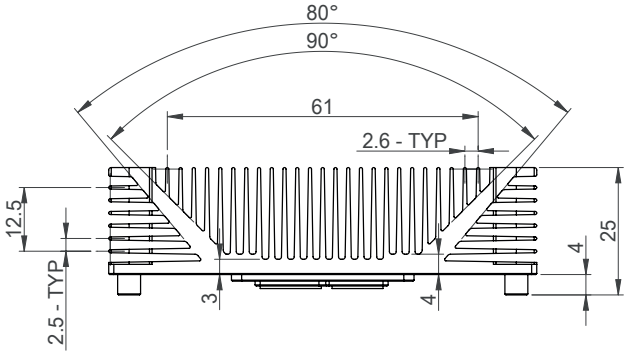


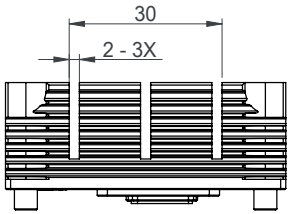
Bare-Die Variants (Part-No.: 049452, 049453)

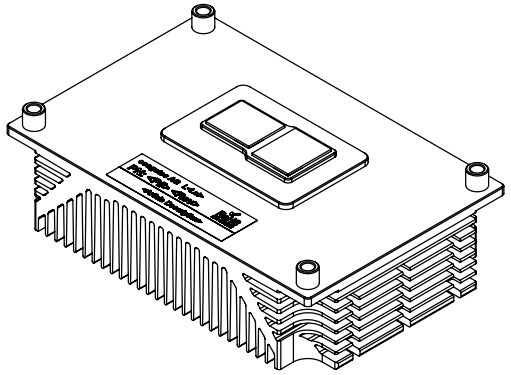


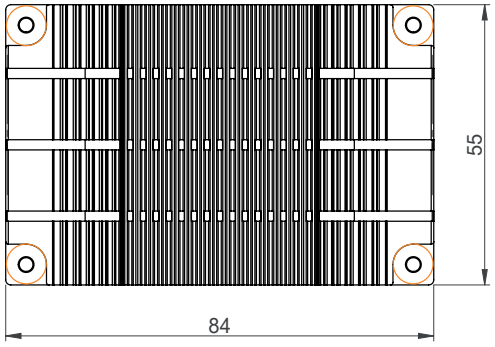
M2.5 x 6 mm threaded standoff for threaded version
or
ø2.7 x 6 mm non-threaded standoff for borehole version











5 Connector Subsystems Rows A, B

The conga-MA7 is connected to the carrier board via a 220-pin connector (COM Express® Type 10 pinout). This connector is broken down into two rows (rows A and B). The following subsystems can be found on conga-MA7 COM Express® connector rows A and B.

5.1 PCI Express

The conga-MA7 offers four PCIe® lanes on the COM Express connector. The lanes are Gen 3 compliant and offer support for full 8 GT/s bandwidth in each direction per x1 link. Default configuration for the lanes is a 4 x1 link. Other configurations are possible as shown in the table below but require a customized BIOS firmware. Contact congatec technical support for more information.

The PCI Express® interface is based on the PCI Express® Specification 3.2 with Gen 1 (2.5 GT/s), Gen 2 (5 GT/s) and Gen 3 (8 GT/s) speed. For more information, refer to Table 18 "General Pupose PCI Express® Lanes Signal Descriptions".

Table 10 PCI Express® Options

	x1	x2	x4
Default	4		
Option	2	1	
Option		2	
Option			1

Note

The options require a customized BIOS.

5.2 Gigabit Ethernet

The conga-MA7 offers a Gigabit Ethernet interface on the COM Express connector via the onboard TI DP83867 Ethernet PHY with support for:

- full- or half-duplex operation at 10/100/1000 Mb/s
- precision clock synchronization
- low jitter and latency
- TSN compliancy
- Wake-on-LAN

The Ethernet interface consists of 4 pairs of low voltage differential pair signals designated from GBE0_MD0± to GBE0_MD3± plus control signals for link activity indicators. These signals can be used to connect to a 10/100/1000 BaseT RJ45 connector with integrated or external isolation magnetics on the carrier board.

5.3 SATA

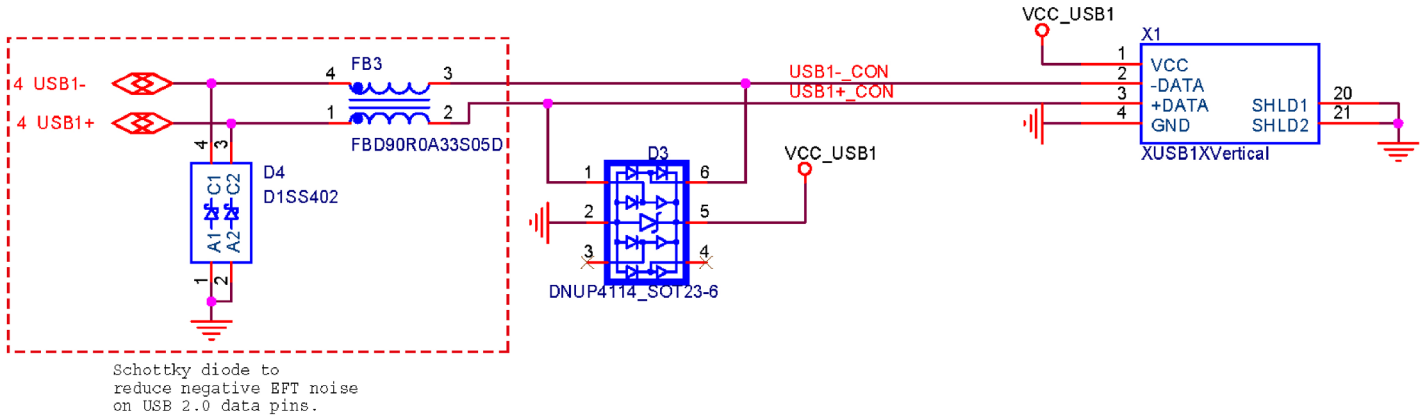
The conga-MA7 offers two SATA interfaces on the COM Express connector via a SATA host controller integrated in the Intel® Elkhart Lake SoC. The controller supports independent DMA operation, AHCI operations and data transfer rates of 1.5 Gb/s, 3.0 Gb/s and 6.0 Gb/s. IDE Mode is not supported.

5.4 USB

The conga-MA7 offers eight USB 2.0 ports and SuperSpeed USB 10Gbps lines for up to two USB 3.1 Gen 2 ports. The USB 3.1 Gen 2 ports are not in addition to the USB 2.0 ports but also support USB 2.0. USB Dual Role is not supported.

Caution

To pass the Electrical Fast Transient (EFT) test, you must add a schottky diode (1SS402 or equivalent) to all USB 2.0 data lanes routed to a connector on your carrier board. The schottky diode must be placed before the common-mode choke as shown below.



5.5 High Definition Audio (HDA) Interface

The conga-MA7 provides an interface to connect an HDA audio codec. Only one external HDA codec is supported.

5.6 Digital Display Interface

The conga-MA7 offers two display interfaces:

- DDI0 supports DisplayPort 1.4
- LVDS_A supports LVDS by default

Optionally, LVDS_A can support eDP instead of LVDS (assembly option).

The supported display combionations are shown below:

Table 11 Display Combination

	DDI0		LVDS_A	
	Display Technology	Max. Resolution	Display Technology	Max. Resolution
Default	DP++	4096x2160 @ 60Hz	LVDS (single channel)	1280x1024 @ 60 Hz
Option	DP++	4096x2160 @ 60Hz	eDP	4096x2160 @ 60Hz

Note

To support the maximum resolution of the DP++, it is recommended to implement a retimer on the carrier board.

5.6.1 DP++

The conga-MA7 offers one Dual-mode DisplayPort (DP++) interface at DDI0 with support for:

- VESA DisplayPort Standard 1.4
- VESA DisplayPort PHY Compliance Test Specification 1.4
- VESA DisplayPort Link Layer Compliance Test Specification 1.4
- Up to 4096x2160 @ 60 Hz (retimer on carrier board is recommended for 4K)
- High-bandwidth Digital Content Protection (HDCP) 2.3 and 1.4
- HD Audio (AC-3 Dolby Digital, Dolby Digital Plus, DTS-HD, LPCM [192 kHz/24 bit, 6 Channel], Dolby TrueHD, DTS-HD Master Audio)

- VESA DSC 1.1
- Multi-Stream Transport (MST)
- Main link of 1, 2, or 4 data lanes
- Color depth of up to 36 bpp
- Spread Spectrum Clock (SSC)
- YCbCR 4:4:4, YCbCR 4:2:0, and RGB color format
- Adaptive sync

Note

To support the maximum resolution of the DP++, a retimer is recommended to be implemented on the carrier board.

5.6.2 LVDS/eDP

The conga-MA7 offers a single channel LVDS interface on the COM Express® connector. The interface is provided by routing the onboard PTN3460 eDP to LVDS bridge to the eDP port of the SoC. The bridge processes the incoming DisplayPort stream, converts the DP protocol to LVDS protocol and transmits the processed stream in LVDS format. The LVDS interface supports:

- ANSI/TIA/EIA-644-A-2001 standard
- Single LVDS bus operation up to 112 mega pixels per second
- Up to 1280x1024 @ 60 Hz resolution in single LVDS bus mode
- Color depth of 18 bits per pixel (bpp) or 24 bpp
- RGB data packing as per JEIDA and VESA data formats
- Pixel clock frequency from 25 MHz to 112 MHz

Optionally, the interface can offer eDP 1.3 (4096x2160 @60Hz) signals instead of LVDS (assembly option).

5.7 SD Card

Optionally, the conga-MA7 can offer a 4-bit SD interface instead of GPIOs (BIOS Setup option). The SDIO interface supports:

- SD Card specification version 3.01 @ 3.3 V Signaling (Default Speed Mode/High Speed Mode)
- SDIO specification version 3.0
- Card Detection (Insertion / Removal) (SD memory card only)

Note

If you disable the eMMC 5.1 controller in the BIOS setup menu, the SD card controller will also be automatically disabled.

5.8 UART/CAN

The conga-MA7 offers two legacy UART ports (SER[0:1]) from the congatec Board Controller (cBC) by default.

Alternatively, SER0 can provide a non-legacy UART port from the SoC (BIOS Setup option). [1]

Alternatively, SER1 can provide a Controller Area Network (CAN) bus (BIOS Setup option) with support for: [2]

- ISO 11898-1 (identical to Bosch CAN protocol specification 2.0 part A,B)
- ISO 11898-4 (Timetriggered communication on CAN)
- CAN FD protocol specification 1.0

Note

1. *Microsoft® Windows® does not support the optional non-legacy UART port because the Intel® PSE UART drivers are currently not available.*
2. *Microsoft® Windows® does not support the optional CAN FD bus because the Intel® driver is currently not available.*

5.9 LPC Bus/eSPI

The conga-MA7 offers the LPC (Low Pin Count) bus by default. The LPC bus corresponds approximately to a serialized ISA bus yet with a significantly reduced number of signals and functionality. Due to the software compatibility to the ISA bus, I/O extensions such as additional serial ports can be easily implemented on an application specific carrier board using this bus. Only certain devices such as Super I/O or TPM chips can be implemented on the carrier board.

The LPC interface is connected to the Enhanced Serial Peripheral Interface (eSPI) controller of the SoC via a Microchip ECE1200 eSPI to LPC bridge by default. Optionally, the conga-MA7 can offer eSPI instead of LPC (assembly option).

Note

The LPC clock frequency is 24 MHz. The LPC_DRQ# signal is not supported. The SERIRQ# signal is programmable to operate with the cBC.

5.10 SPI Bus

The conga-MA7 offers a Serial Peripheral Interface (SPI) for an external 3.3V 32 Mbyte BIOS Flash device powered from the standby rail.

Optionally, the SPI can be connected to the PCH SPI1 of the SoC instead to support other SPI devices (assembly option).

5.11 I²C Bus

The conga-MA7 offers an Inter-Integrated Circuit (I^2C) bus inteface connected to the congatec Board Controller (cBC). The bus has 2.2k ohm pull-ups resistors on the CLK and DATA signals and is powered from standby 3.3V.

5.12 SMBus

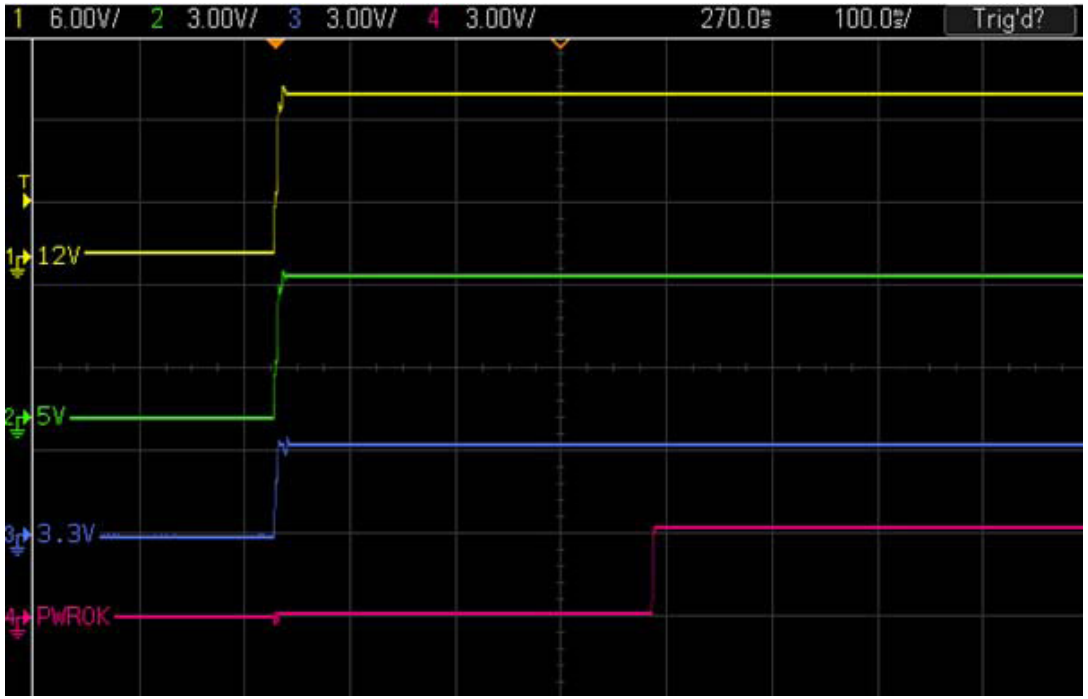
The conga-MA7 provides an SMBus connected to the congatec Board Controller (cBC) by default. It is an I²C bus variant for system management functions. The bus is powered from standby 3.3V and has 2.2k ohm pull-ups resistors on the CLK and DATA signals. ALERT# signal has a 10k ohm pull-up resistor.

Optionally, the SMBus can be connected to the SoC SMBus via an isolation switch instead (BIOS setup option).

5.13 Power Control

PWR_OK

Power OK from main power supply or carrier board voltage regulator circuitry. A high value indicates that the power is good and the module can start its onboard power sequencing. Carrier board hardware must drive this signal low until all power rails and clocks are stable. Releasing PWR_OK too early or not driving it low at all can cause numerous boot up problems. It is a good design practice to delay the PWR_OK signal a little (typically 100ms) after all carrier board power rails are up, to ensure a stable system. See screenshot below.



Note

The module is kept in reset as long as the PWR_OK is driven by carrier board hardware.

It is strongly recommended that the carrier board hardware drives the signal low until it is safe to let the module boot-up.

The three typical usage scenarios for a carrier board design are:

- Connect PWR_OK to the “power good” signal of an ATX type power supply.
- Connect PWR_OK to the last voltage regulator in the chain on the carrier board.
- Simply pull PWR_OK with a 1k resistor to the carrier board 3.3V power rail.

With this solution, you must make sure that by the time the 3.3V is up, all carrier board hardware is fully powered and all clocks are stable.

The conga-MA7 provides support for controlling ATX-style power supplies. When not using an ATX power supply then the conga-MA7's pins SUS_S3/PS_ON, 5V_SB, and PWRBTN# should be left unconnected.

SUS_S3#/PS_ON#

The SUS_S3#/PS_ON# (pin A15 on the COM Express connector) signal is an active-low output that can be used to turn on the main outputs of an ATX-style power supply. In order to accomplish this the signal must be inverted with an inverter/transistor that is supplied by standby voltage and is located on the carrier board.

PWRBTN#

When using ATX-style power supplies PWRBTN# (pin B12 on the COM Express connector) is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. This signal is internally pulled up to 3V_SB using a 20k resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

Power Supply Implementation Guidelines

Input power of 4.75 - 20 volt is the sole operational power source for the conga-MA7. The remaining necessary voltages are internally generated on the module using onboard voltage regulators. A carrier board designer should be aware of the following important information when designing a power supply for a conga-MA7 application:

- It has also been noticed that on some occasions, problems occur when using a power supply that produces non monotonic voltage when powered up. The problem is that some internal circuits on the module (e.g. clock-generator chips) will generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused resulting in a malfunction. It must be mentioned that this problem is quite rare but has been observed in some mobile power supply applications. The best way to ensure that this problem is not encountered is to observe the power supply rise waveform through the use of an oscilloscope to determine if the rise is indeed monotonic and does not have any dips. This should be done during the power supply qualification phase therefore ensuring that the above mentioned problem doesn't arise in the application. For more information, see the “Power Supply Design Guide for Desktop Platform Form Factors” document at www.intel.com.

Inrush and Maximum Current Peaks on VCC_5V_SB and VCC

The inrush current on the conga-MA7 VCC_5V_SB power rail can go up as high as 6.13 A and as high as 27.94 A on VCC power rail (12 V) within a short time (approx. 150µs) and with a voltage rise time of 100µs. Sufficient decoupling capacitance must be implemented on the carrier board to ensure proper power-up sequencing.

5.14 Power Management

ACPI 5.0 compliant with battery support. Also supports Suspend to RAM (S3).

6 Additional Features

6.1 Integrated Real-Time Hypervisor

The RTS Hypervisor is integrated into the congatec firmware on the conga-MA7 by default. With the RTS Hypervisor, you can consolidate functionality that previously required multiple dedicated system on a single x86 hardware platform.

The integrated RTS Hypervisor offers a 30-day free evaluation license. The 30-day evaluation starts when the customer receives the x86-based modules. To access the full package, contact congatec Sales team via the online "Request Quote" button for your particular product at https://www.congatec.com/en/products/hypervisor-products/.

To activate the RTS Hypervisor, change the “Boot Device” in the BIOS setup menu to “Integrated RTS Hypervisor”.

1. Press F2 or DEL during POST to enter the BIOS setup menu.
2. Go to the Boot tab to enter the Boot setup screen.
3. Select “Integrated RTS Hypervisor" as “1st Boot Device”.
4. Go to the Save & Exit tab and select “Save Changes and Exit”.

For more information about the integrated Hypervisor, see the congatec Application Note AN56_Hypervisor_on_Module.pdf on the congatec website at https://www.congatec.com/en/support/application-notes/.

Note

1. *The configuration steps and the BIOS setup menu above are valid for "Type Based Boot Priority". For "UEFI Boot Priority", the BIOS setup menu may differ.*
2. *The Real-Time Operating System images, driver packages for the General-Purpose Operating System and the installation procedures for the Operating Systems are available for download under the "Technical information" section, in the restricted area of congatec website at www.congatec.com/login. If you require login access, contact your local sales representative.*

6.2 Onboard Interfaces

6.2.1 eMMC

The conga-MA7 offers an onboard eMMC 5.1 HS400 storage device with up to 64 GB storage capacity. The default eMMC storage capacity of each conga-MA7 variant is listed in section 1.1 "Options Information". Changes to the onboard eMMC may occur during the lifespan of the module in order to keep up with the rapidly changing eMMC technology. The performance of the newer eMMC may vary depending on the eMMC technology.

Optionally, the conga-MA7 can offer an eMMC with up to up to 256 GB storage capacity (assembly option).

Note

1. *For adequate operation of the eMMC, ensure that at least 15 % of the eMMC storage is reserved for vendor-specific functions.*
2. *If you disable the eMMC 5.1 controller in the BIOS setup menu, the SD card controller will also be automatically disabled.*

6.2.2 Security Features

The conga-MA7 offers a discrete TPM 2.0 (Infineon SLB9670VQ2.0).

6.3 congatec Board Controller (cBC)

The conga-MA7 is equipped with a microcontroller. The microcontroller plays an important role for most of the congatec BIOS features. By isolating some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, the microcontroller increases the performance and reliability of the BIOS features, even during low power mode. In addition, it ensures the congatec embedded feature set is compatible amongst all congatec modules.

Some of the features offered by the cBC are described in the following sub-sections below.

6.3.1 Board Information

The cBC provides a rich data-set of manufacturing and board information such as serial number, EAN number, hardware and firmware revisions, and so on. It also keeps track of dynamically changing data like runtime meter and boot counter.

6.3.2 Fan Control

The conga-MA7 has additional signals and functions to further improve system management. One of these signals is an output signal called FAN_PWMOUT that allows system fan control using a PWM (Pulse Width Modulation) output. Additionally, there is an input signal called FAN_TACHIN that provides the ability to monitor the system's fan RPMs (revolutions per minute). This signal must receive two pulses per revolution in order to produce an accurate reading. For this reason, a two pulse per revolution fan or similar hardware solution is recommended.

Note

For the correct fan control (FAN_PWMOUT, FAN_TACHIN) implementation, see the COM Express® Design Guide.

6.3.3 Power Loss Control

The cBC provides the power loss control feature. The power loss control feature determines the behaviour of the system after an AC power loss occurs. This feature applies to systems with ATX-style power supplies which support standby power rail.

The term "power loss" implies that all power sources, including the standby power are lost (G3 state). Once power loss (transition to G3) or shutdown (transition to S5) occurs, the board controller continuously monitors the standby power rail. If the standby voltage remains stable for 30 seconds, the cBC assumes the system was switched off properly. If the standby voltage is no longer detected within 30 seconds, the module considers this an AC power loss condition.

The power loss control feature has three different modes that define how the system responds when standby power is restored after a power loss occurs. The modes are:

- Turn On: The system is turned on after a power loss condition
- Remain Off: The system is kept off after a power loss condition
- Last State: The board controller restores the last state of the system before the power loss condition

Note

1. *If a power loss condition occurs within 30 seconds after a regular shutdown, the cBC may incorrectly set the last state to "ON".*
2. *The settings for power loss control have no effect on systems with AT-style power supplies which do not support standby power rail.*
3. *The 30 seconds monitoring cycle applies only to the "Last State" power loss control mode.*

6.3.4 Watchdog

The conga-MA7 is equipped with a multi stage watchdog solution that is triggered by software. The COM Express® Specification does not provide support for external hardware triggering of the watchdog; therefore, the conga-MA7 does not support external hardware triggering.

For more information, refer to the application note "AN03 Watchdog" at www.congatec.com.

Note

The conga-QA7 does not support the watchdog NMI mode.

6.3.5 Enhanced Soft-Off State

The conga-MA7 supports an enhanced Soft-Off state (S5e)—a congatec proprietary low-power Soft-Off state. In this state, the CPU module switches off almost all the onboard logic in order to reduce the power consumption to absolute minimum (approximately 1.4 mA).

The S5e supports power button, sleep button and SMBALERT# wake events. Refer to congatec application note AN36_S5e_Implementation.pdf for detailed description of the S5e state.

6.3.6 General Purpose Input/Output

The conga-MA7 offers four GPI and four GPO via the congatec Board Controller (cBC) by default. Alternatively, the conga-MA7 can offer an SDIO interface instead of the GPIOs (BIOS Setup option).

6.4 OEM BIOS Customization

The conga-MA7 is equipped with congatec Embedded BIOS, which is based on American Megatrends Inc. Aptio UEFI firmware. The congatec Embedded BIOS allows system designers to modify the BIOS. For more information about customizing the congatec Embedded BIOS, refer to the congatec System Utility user's guide CGUTLm1x.pdf on the congatec website at www.congatec.com or contact technical support.

The supported customization features are described in the following sub-sections.

6.4.1 OEM Default Settings

This feature allows system designers to create and store their own BIOS default configuration. Customized BIOS development by congatec for OEM default settings is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_OEM_Default_Map.pdf on the congatec website for details on how to add OEM default settings to the congatec Embedded BIOS.

6.4.2 OEM Boot Logo

This feature allows system designers to replace the standard text output displayed during POST with their own BIOS boot logo. Customized BIOS development by congatec for OEM Boot Logo is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_And_Add_Bootlogo.pdf on the congatec website for details on how to add OEM boot logo to the congatec Embedded BIOS.

6.4.3 OEM POST Logo

This feature allows system designers to replace the congatec POST logo displayed in the upper left corner of the screen during BIOS POST with their own BIOS POST logo. Use the congatec system utility CGUTIL 1.5.4 or later to replace/add the OEM POST logo.

6.4.4 OEM BIOS Code/Data

With the congatec embedded BIOS, it used to be possible for system designers to add their own code to the BIOS POST process. This feature is no longer supported with the new UEFI based firmware.

6.4.5 OEM DXE Driver

This feature allows designers to add their own UEFI DXE driver to the congatec embedded BIOS. Contact congatec technical support for more information on how to add an OEM DXE driver.

6.5 congatec Battery Management Interface

In order to facilitate the development of battery powered mobile systems based on embedded modules, congatec has defined an interface for the exchange of data between a x86 CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (e.g. charge state of the battery, information about the battery, alarms/events for certain battery states, ...) without the need for any additional modifications to the system BIOS.

In addition to the ACPI-compliant Control Method Battery mentioned above, the latest versions of the conga-MA7 BIOS and board controller firmware also support the LTC1760 battery manager from Linear Technology and a battery only solution (no charger). All three battery solutions are supported on the I2C bus and the SMBus. This gives the system designer more flexibility when choosing the appropriate battery sub-system.

For more information about the supported Battery Management Interface contact your local congatec sales representative.

6.6 API Support (CGOS)

In order to benefit from the above mentioned non-industry standard feature set, congatec provides an API that allows application software developers to easily integrate all these features into their code. The CGOS API (congatec Operating System Application Programming Interface) is the congatec proprietary API that is available for all commonly used Operating Systems such as Win32, Win64, Linux. The architecture of the CGOS API driver provides the ability to write application software that runs unmodified on all congatec CPU modules. All the hardware related code is contained within the congatec embedded BIOS on the module. See section 1.1 of the CGOS API software developers guide at www.congatec.com.

6.7 Suspend to Ram

The Suspend to RAM feature is available on the conga-MA7.

7 conga Tech Notes

The conga-MA7 has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features.

7.1 Intel® Elkhart Lake SoC Features

7.1.1 Processor Core

The SoC features Dual or Quad 3-way Supersclar, Out-of-Order Execution processor cores. Some of the features supported by the core are:

- Intel® 64 architecture
- Intel® Streaming SIMD Extensions
- Support for Intel® VTx-2 and VT-d
- Thermal management support vial Intel® Thermal Monitor
- Uses Programmable Service Engine Interrupt Routing
- Uses 10 nm process technology

Note

Intel® Hyper-Threading technology is not supported (four cores execute four threads)

7.1.1.1 Intel Virtualization Technology

Intel® Virtualization Technology (Intel® VT) makes a single system appear as multiple independent systems to software. This allows multiple, independent operating systems to run simultaneously on a single system. Intel® VT comprises technology components to support virtualization of platforms based on Intel architecture microprocessors and chipsets. Intel® Virtualization Technology for IA-32, Intel® 64 and Intel® Architecture Intel® VT-x added hardware support in the processor to improve the virtualization performance and robustness.

RTS Real-Time Hypervisor supports Intel® VT and is verified on all current congatec x86 hardware.

Note

congatec supports RTS Hypervisor.

7.1.1.2 AHCI

The SoC provides hardware support for Advanced Host Controller Interface (AHCI), a programming interface for SATA host controllers. Platforms supporting AHCI may take advantage of performance features such as no master/slave designation for SATA devices (each device is treated as a master) and hardware-assisted native command queuing. AHCI also provides usability enhancements such as Hot-Plug.

7.1.1.3 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system's thermal management. This results in the operating system having the ability to take control of the operating environment by implementing cooling decisions according to the demands put on the CPU by the application.

The conga-MA7 ACPI thermal solution offers two different cooling policies:

- Passive Cooling

When the temperature in the thermal zone must be reduced, the operating system can decrease the power consumption of the processor by throttling the processor clock. One of the advantages of this cooling policy is that passive cooling devices (in this case the processor) do not produce any noise. Use the "passive cooling trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start or stop the passive cooling procedure.

- Critical Trip Point

If the temperature in the thermal zone reaches a critical point then the operating system will perform a system shut down in an orderly fashion in order to ensure that there is no damage done to the system as result of high temperatures. Use the "critical trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to shut down the system.

Note

The end user must determine the cooling preferences for the system by using the setup nodes in the BIOS setup program to establish the appropriate trip points.

If passive cooling is activated and the processor temperature is above the trip point the processor clock is throttled. See section 12 of the ACPI Specification 2.0 C for more information about passive cooling.

7.2 ACPI Suspend Modes and Resume Events

conga-MA7 supports S3 (STR= Suspend to RAM). The BIOS does not support S4 (Suspend to Disk).

The table below lists the "Wake Events" that resume the system from S3 unless otherwise stated in the "Conditions/Remarks" column:

Table 12 Wake Events resuming system from S3

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S3-S5.
Onboard LAN Event	Device driver must be configured for Wake On LAN support.
PCI Express WAKE#	Wakes unconditionally from S3-S5.
PME#	Activate the wake up capabilities of a PCI device using Windows Device Manager configuration options for this device OR set Resume On PME# to Enabled in the Power setup menu.
USB Mouse/Keyboard Event	When Standby mode is set to S3, USB Hardware must be powered by standby power source. Set USB Device Wakeup from S3/S4 to ENABLED in the ACPI setup menu (if setup node is available in BIOS setup program). In Device Manager look for the keyboard/mouse devices. Go to the Power Management tab and check 'Allow this device to bring the computer out of standby'.
RTC Alarm	Activate and configure Resume On RTC Alarm in the Power setup menu. Only available in S5.
Watchdog Power Button Event	Wakes unconditionally from S3-S5.

8 Signal Descriptions and Pinout Tables

The following section describes the signals found on COM Express® Type 10 connectors used for congatec GmbH modules. The pinout of the modules complies with COM Express® Type 10 Rev. 3.0.

The table below describes the terminology used in this section for the Signal Description tables. The PU/PD column indicates if a COM Express® module pull-up or pull-down resistor has been used. If the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented by congatec.

The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

Note

The Signal Description tables do not list internal pull-ups or pull-downs implemented by the chip vendors, only pull-ups or pull-downs implemented by congatec are listed. For information about the internal pull-ups or pull-downs implemented by the chip vendors, refer to the respective chip's datasheet.

Table 13 Signal Tables Terminology Descriptions

Term	Description
PU	congatec implemented pull-up resistor
PD	congatec implemented pull-down resistor
I/O 3.3V	Bi-directional signal 3.3V
I/O 5V	Bi-directional signal 5V
I 3.3V	Input 3.3V
I 5V	Input 5V
I/O 3.3VSB	Input 3.3V active in standby state
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
OD	Open drain output pin
P	Power input pin
DDC	Display Data Channel
PCIE	In compliance with PCI Express Base Specification, Revision 2.0
SATA	In compliance with Serial ATA specification Revision 2.6 and 3.0.
REF	Reference voltage output. May be sourced from a module power plane.
PDS	Pull-down strap. A module output pin that is either tied to GND or is not connected. Used to signal module capabilities (pinout type) to the Carrier Board.

8.1 COM Express® Connector Pinout

Table 14 COM Express® Connector Pinouts

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A1	GND(FIXED)	B1	GND(FIXED)	A56	RSVD	B56	RSVD
A2	GBE0_MDI3-	B2	GBE0_ACT#	A57	GND	B57	GPO2
A3	GBE0_MDI3+	B3	LPC_FRAME#/ ESPI_CS0# [2]	A58	PCIE_TX3+	B58	PCIE_RX3+
A4	GBE0_LINK100#	B4	LPC_AD0/ ESPI_IO_0 [2]	A59	PCIE_TX3-	B59	PCIE_RX3-
A5	GBE0_LINK1000#	B5	LPC_AD1/ ESPI_IO_1 [2]	A60	GND(FIXED)	B60	GND(FIXED)
A6	GBE0_MDI2-	B6	LPC_AD2/ ESPI_IO_2 [2]	A61	PCIE_TX2+	B61	PCIE_RX2+
A7	GBE0_MDI2+	B7	LPC_AD3/ ESPI_IO_3 [2]	A62	PCIE_TX2-	B62	PCIE_RX2-
A8	GBE0_LINK#	B8	LPC_DRQ0# [1]/ ESPI_ALERT0# [2]	A63	GPI1	B63	GPO3
A9	GBE0_MDI1-	B9	LPC_DRQ1# [1]/ ESPI_ALERT1# [2]	A64	PCIE_TX1+	B64	PCIE_RX1+
A10	GBE0_MDI1+	B10	LPC_CLK/ ESPI_CK [2]	A65	PCIE_TX1-	B65	PCIE_RX1-
A11	GND(FIXED)	B11	GND(FIXED)	A66	GND	B66	WAKE0#
A12	GBE0_MDI0-	B12	PWRBTN#	A67	GPI2	B67	WAKE1#
A13	GBE0_MDI0+	B13	SMB_CK	A68	PCIE_TX0+	B68	PCIE_RX0+
A14	GBE0_CTREF [1]	B14	SMB_DAT	A69	PCIE_TX0-	B69	PCIE_RX0-
A15	SUS_S3#	B15	SMB_ALERT#	A70	GND(FIXED)	B70	GND(FIXED)
A16	SATA0_TX+	B16	SATA1_TX+	A71	eDP_TX2+ [2]/ LVDS_A0+	B71	DDI0_PAIR0+
A17	SATA0_TX-	B17	SATA1_TX-	A72	eDP_TX2- [2]/ LVDS_A0-	B72	DDI0_PAIR0-
A18	SUS_S4#	B18	SUS_STAT# / ESPI RESET# [2]	A73	eDP_TX1+ [2]/ LVDS_A1+	B73	DDI0_PAIR1+
A19	SATA0_RX+	B19	SATA1_RX+	A74	eDP_TX1- [2]/ LVDS_A1-	B74	DDI0_PAIR1-
A20	SATA0_RX-	B20	SATA1_RX-	A75	eDP_TX0+ [2]/ LVDS_A2+	B75	DDI0_PAIR2+
A21	GND(FIXED)	B21	GND(FIXED)	A76	eDP_TX0- [2]/ LVDS_A2-	B76	DDI0_PAIR2-
A22	USB_SSRX0-	B22	USB_SSTX0-	A77	eDP_VDD_EN [2]/ LVDS_VDD_EN	B77	DDI0_PAIR4+ [1]
A23	USB_SSRX0+	B23	USB_SSTX0+	A78	LVDS_A3+	B78	DDI0_PAIR4- [1]

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A24	SUS_S5#	B24	PWR_OK	A79	LVDS_A3-	B79	eDP_BKLT_EN [2]/ LVDS_BKLT_EN
A25	USB_SSRX1-	B25	USB_SSTX1-	A80	GND(FIXED)	B80	GND(FIXED)
A26	USB_SSRX1+	B26	USB_SSTX1+	A81	eDP_TX3+/ LVDS_A_CK+	B81	DDI0_PAIR3+
A27	BATLOW#	B27	WDT	A82	eDP_TX3- [2]/ LVDS_A_CK-	B82	DDI0_PAIR3-
A28	(S)ATA_ACT#	B28	HDA_SDIN2 [1]	A83	eDP_AUX+ [2]/ LVDS_I2C_CK	B83	eDP_BKLT_CTRL [2]/ LVDS_BKLT_CTRL
A29	HDA_SYNC	B29	HDA_SDIN1 [1]	A84	eDP_AUX- [2]/ LVDS_I2C_DAT	B84	VCC_5V_SBY
A30	HDA_RST#	B30	HDA_SDIN0	A85	GPI3	B85	VCC_5V_SBY
A31	GND(FIXED)	B31	GND(FIXED)	A86	RSVD	B86	VCC_5V_SBY
A32	HDA_BITCLK	B32	SPKR	A87	eDP_HPD [2]	B87	VCC_5V_SBY
A33	HDA_SDOUT	B33	I2C_CK	A88	PCIE_CLK_REF+	B88	BIOS_DIS1#
A34	BIOS_DIS0#/ ESPI_SAFS [1]	B34	I2C_DAT	A89	PCIE_CLK_REF-	B89	DDI0_HPD
A35	THRMTRIP#	B35	THRM#	A90	GND(FIXED)	B90	GND(FIXED)
A36	USB6-	B36	USB7	A91	SPI_POWER	B91	DDI0_PAIR5+ [1]
A37	USB6+	B37	USB7+	A92	SPI_MISO	B92	DDI0_PAIR5- [1]
A38	USB_6_7_OC#	B38	USB_4_5_OC#	A93	GPO0	B93	DDI0_PAIR6+ [1]
A39	USB4-	B39	USB5-	A94	SPI_CLK	B94	DDI0_PAIR6- [1]
A40	USB4+	B40	USB5+	A95	SPI_MOSI	B95	DDI0_DDC_AUX_SEL
A41	GND(FIXED)	B41	GND(FIXED)	A96	TPM_PP [1]	B96	USB7_HOST_PRSNT
A42	USB2-	B42	USB3-	A97	TYPE10#	B97	SPI_CS#
A43	USB2+	B43	USB3+	A98	SER0_TX	B98	DDI0_CTRLCLK_AUX+
A44	USB_2_3_OC#	B44	USB_0_1_OC#	A99	SER0_RX	B99	DDI0_CTRLDATA_AUX-
A45	USB0-	B45	USB1-	A100	GND(FIXED)	B100	GND(FIXED)
A46	USB0+	B46	USB1+	A101	SER1_TX	B101	FAN_PWMOUT
A47	VCC_RTC	B47	ESPI_EN# [2]	A102	SER1_RX	B102	FAN_TACHIN
A48	RSVD	B48	USB0_HOST_PRSNT [2]	A103	LID#	B103	SLEEP#
A49	GBE0_SDP	B49	SYS_RESET#	A104	VCC_12V	B104	VCC_12V
A50	LPC_SERIRQ/ ESPI_CS1# [2]	B50	CB_RESET#	A105	VCC_12V	B105	VCC_12V
A51	GND(FIXED)	B51	GND(FIXED)	A106	VCC_12V	B106	VCC_12V
A52	RSVD	B52	RSVD	A107	VCC_12V	B107	VCC_12V
A53	RSVD	B53	RSVD	A108	VCC_12V	B108	VCC_12V
A54	GPI0	B54	GPO1	A109	VCC_12V	B109	VCC_12V
A55	RSVD	B55	RSVD	A110	GND(FIXED)	B110	GND(FIXED)

1. *Not supported*
2. *Assembly option*

8.2 COM Express® Connector Signal Descriptions

Table 15 High Definition Audio Link Signals Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
HDA_RST#	A30	High Definition Audio Reset: This signal is the master hardware reset to external codec(s).	O 3.3V	PD 75K	
HDA_SYNC	A29	High Definition Audio Sync: This signal is a 48 kHz fixed rate sample sync to the codec(s). It is also used to encode the stream number.	O 3.3V		
HDA_BITCLK	A32	High Definition Audio Bit Clock Output: This signal is a 24.000 MHz serial data clock generated by the Intel® High Definition Audio controller.	O 3.3V	PD 75K	
HDA_SDOUT	A33	High Definition Audio Serial Data Out: This signal is the serial TDM data output to the codec. This serial output is double-pumped for a bit rate of 48 Mb/s for Intel® High Definition Audio.	O 3.3V		
HDA_SDIN[0]	B30	High Definition Audio Serial Data In [0]: This signal is a serial TDM data input from the codec. The serial input is single-pumped for a bit rate of 24 Mb/s for Intel® High Definition Audio.	I/O 3.3V		HDA_SDIN[2:1] are not connected.

Table 16 Gigabit Ethernet Signal Descriptions

Gigabit Ethernet	Pin #	Description				I/O	PU/PD	Comment
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	A13 A12 A10 A9 A7 A6 A3 A2	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10 Mbit/sec modes. Some pairs are unused in some modes according to the following:				I/O Analog		Twisted pair signals for external transformer.
			1000	100	10			
		MDI[0]+/-	B1_DA+/-	TX+/-	TX+/-			
		MDI[1]+/-	B1_DB+/-	RX+/-	RX+/-			
		MDI[2]+/-	B1_DC+/-					
		MDI[3]+/-	B1_DD+/-					
GBE0_ACT#	B2	Gigabit Ethernet Controller 0 activity indicator, active low.				O 3.3VSB		
GBE0_LINK#	A8	Gigabit Ethernet Controller 0 link indicator, active low.				O 3.3VSB		indicates only LINK100 and LINK1000
GBE0_LINK100#	A4	Gigabit Ethernet Controller 0 100 Mbit/sec link indicator, active low.				O 3.3VSB		
GBE0_LINK1000#	A5	Gigabit Ethernet Controller 0 1000 Mbit/sec link indicator, active low.				O 3.3VSB		
GBE0_CTREF	A14	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the module. In the case in which the reference is shorted to ground, the current shall be limited to 250mA or less.						Not connected
GBE0_SDP	A49	Gigabit Ethernet Controller 0 Software-Definable Pin. Can also be used for IEEE1588 support such as a 1pps signal. See section 4.3.5 "SDP Pins" of the COM Express 3.0 Specification for details.				I/O		

Table 17 Serial ATA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_RX+ SATA0_RX-	A19 A20	Serial ATA channel 0, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 3.2
SATA0_TX+ SATA0_TX-	A16 A17	Serial ATA channel 0, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 3.2
SATA1_RX+ SATA1_RX-	B19 B20	Serial ATA channel 1, Receive Input differential pair.	I SATA		Supports Serial ATA specification, Revision 3.2
SATA1_TX+ SATA1_TX-	B16 B17	Serial ATA channel 1, Transmit Output differential pair.	O SATA		Supports Serial ATA specification, Revision 3.2
S_ATA_ACT#	A28	Serial ATA activity indicator, active low.	O 3.3V		Up to 10mA

Table 18 General Pupose PCI Express® Lanes Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express channel 0, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express channel 0, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express channel 1, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express channel 1, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express channel 2, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express channel 2, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express channel 3, Receive Input differential pair.	I PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express channel 3, Transmit Output differential pair.	O PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCI Express Reference Clock output for all PCI Express lanes.	O PCIE		A PCI Express Gen2/3 compliant clock buffer chip must be used on the carrier board if more than one PCI Express device is designed in.

Table 19 USB Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB0+ USB0-	A46 A45	USB Port 0 differential data pairs	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB1+ USB1-	B46 B45	USB Port 1 differential data pairs	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB2+ USB2-	A43 A42	USB Port 2 differential data pairs	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB3+ USB3-	B43 B42	USB Port 3 differential data pairs	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB4+ USB4-	A40 A39	USB Port 4 differential data pairs	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB5+ USB5-	B40 B39	USB Port 5 differential data pairs	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB6+ USB6-	A37 A36	USB Port 6 differential data pairs	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1
USB7+ USB7-	B37 B36	USB Port 7 differential data pairs	I/O		USB 2.0 compliant. Backwards compatible to USB 1.1. USB Dual Role is not supported..
USB0_HOST_PRSNT	B48	Module USB client may detect the presence of a USB host on USB0. A high value indicates that a host is present.			not connected
USB7_HOST_PRSNT	B96	Module USB client may detect the presence of a USB host on USB7. A high value indicates that a host is present.			not connected
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_4_5_OC#	B38	USB over-current sense, USB ports 4 and 5. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_6_7_OC#	A38	USB over-current sense, USB ports 6 and 7. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3VSB	Do not pull this line high on the carrier board.
USB_SSTX0+ USB_SSTX0-	B23 B22	Additional transmit signal differential pairs for the SuperSpeed USB data path. Supports up to SuperSpeed USB 10Gbps.	O USB-SS		SuperSpeed USB 10Gbps requires a retimer on the carrier board. The speed can be limited to SuperSpeed USB 5Gbps in the BIOS Setup.
USB_SSTX1+ USB_SSTX1-	B26 B25	Additional transmit signal differential pairs for the SuperSpeed USB data path. Supports up to SuperSpeed USB 10Gbps.	O USB-SS		
USB_SSRX0+ USB_SSRX0-	A23 A22	Additional receive signal differential pairs for the SuperSpeed USB data path. Supports up to SuperSpeed USB 10Gbps.	I USB-SS		
USB_SSRX1+ USB_SSRX1-	A26 A25	Additional receive signal differential pairs for the SuperSpeed USB data path. Supports up to SuperSpeed USB 10Gbps.	I USB-SS		

Table 20 LVDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LVDS_A0+ eDP_TX2+	A71	LVDS Channel A differential pair 0 Embedded Display Port channel 0 differential pair 2	O LVDS O eDP		LVDS (default) Assembly option: eDP
LVDS_A0- eDP_TX2-	A72	LVDS Channel A differential pair 0 Embedded Display Port channel 0 differential pair 2	O LVDS O eDP		LVDS (default) Assembly option: eDP
LVDS_A1+ eDP_TX1+	A73	LVDS Channel A differential pair 1 Embedded Display Port channel 0 differential pair 1	O LVDS O eDP		LVDS (default) Assembly option: eDP
LVDS_A1- eDP_TX1-	A74	LVDS Channel A differential pair 1 Embedded Display Port channel 0 differential pair 1	O LVDS O eDP		LVDS (default) Assembly option: eDP
LVDS_A2+ eDP_TX0+	A75	LVDS Channel A differential pair 2 Embedded Display Port channel 0 differential pair 0	O LVDS O eDP		LVDS (default) Assembly option: eDP
LVDS_A2- eDP_TX0-	A76	LVDS Channel A differential pair 2 Embedded Display Port channel 0 differential pair 0	O LVDS O eDP		LVDS (default) Assembly option: eDP
LVDS_A3+	A78	LVDS Channel A differential pair 3	O LVDS		
LVDS_A3-	A79	LVDS Channel A differential pair 3	O LVDS		
LVDS_A_CK+ eDP_TX3+	A81	LVDS Channel A differential clock Embedded Display Port channel 0 differential pair 3	O LVDS O eDP		LVDS (default) Assembly option: eDP
LVDS_A_CK- eDP_TX3-	A82	LVDS Channel A differential clock Embedded Display Port channel 0 differential pair 3	O LVDS O eDP		LVDS (default) Assembly option: eDP
LVDS_VDD_EN eDP_VDD_EN	A77	Panel power enable	O 3.3V		LVDS (default) Assembly option: eDP
LVDS_BKLT_EN eDP_BKLT_EN	B79	Panel backlight enable	O 3.3V		LVDS (default) Assembly option: eDP
LVDS_BKLT_CTRL eDP_BKLT_CTRL	B83	Panel backlight brightness control	O 3.3V		LVDS (default) Assembly option: eDP
LVDS_I2C_CK eDP_AUX+	A83	DDC lines used for flat panel detection and control. Embedded Display Port AUX channel pair	I/O 3.3V I/O eDP	LVDS PU 2k2 3.3V	LVDS (default) Assembly option: eDP
LVDS_I2C_DAT eDP_AUX-	A84	DDC lines used for flat panel detection and control. Embedded Display Port AUX channel pair	I/O 3.3V I/O eDP	LVDS PU 2k2 3.3V	LVDS (default) Assembly option: eDP

Table 21 LPC/eSPI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LPC_AD[0:3] / ESPI_IO_[0:3]	B4-B7	LPC multiplexed address, command and data bus. eSPI Master Data Input / Outputs.	I/O 3.3V I/O 1.8V		LPC (default) Assembly option: eSPI
LPC_FRAME# / ESPI_CS0#	B3	LPC frame indicates the start of an LPC cycle. eSPI Master Chip Select Outputs Driving Chip Select0# low selects eSPI slave. Each eSPI slave is connected to a dedicated Chip Select # pin.	O 3.3V O 1.8V		LPC (default) Assembly option: eSPI
LPC_CLK / ESPI_CK	B10	LPC clock output (24MHz). This pin provides the reference timing for all the serial input and output operations.	O 3.3V O 1.8V		LPC (default) Assembly option: eSPI
LPC_DRQ[0:1]# / ESPI_ALERT[0:1]#	B8-B9	LPC serial DMA request . eSPI pins used by eSPI slave to request service from the eSPI master.	I 3.3V I 1.8V		not connected (default) Assembly option: eSPI
LPC_SERIRQ / ESPI_CS1#	A50	LPC serial interrupt. Low selects a particular eSPI slave for the transaction. Each of the eSPI slaves is connected to a dedicated Chip Select pin.	I/O OD 3.3V O 1.8V		LPC (default) Assembly option: eSPI
SUS_STAT# / ESPI_RESET#	B18	Indicates the system will enter a low power state soon. Used to notify LPC devices. Reset eSPI interface for both master and slaves. Typically driven from eSPI master to eSPI slaves.	O 3.3VSB O 1.8V		SUS_STAT# (default) Assembly option: eSPI
ESPI_EN#	B47	This signal is used by the Carrier to indicate the operating mode of the LPC/eSPI bus. If left unconnected on the carrier, LPC mode (default) is selected. If pulled to GND on the carrier, eSPI mode is selected. This signal is pulled to a logic high on he module through a resistor. The Carrier should only float his line or pull it low.	I 3.3V	PU 10k	not connected (default) Assembly option: eSPI
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device.	I 3.3VSB	PU 10k 3.3VSB	Carrier shall pull to GND or leave no-connect.
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device. Ground to select external SPI device. Pull high or leave no-connect to select on-module BIOS flash	I 3.3VSB	PU 10k 3.3VSB	Carrier shall pull to GND or leave no-connect

Table 22 SPI Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPI_CS#	B97	Chip select for carrier board SPI.	O 3.3VSB	PU 100k	
SPI_MISO	A92	Master Input Slave Output: SPI output data from carrier board SPI device to module.	I 3.3VSB		
SPI_MOSI	A95	Master Output Slave Input: SPI output data from module to carrier board SPI.	O 3.3VSB	PU 20k	
SPI_CLK	A94	Clock from module to carrier board SPI BIOS flash.	O 3.3VSB	PD 75k	
SPI_POWER	A91	Power source for carrier board SPI BIOS flash. SPI_POWER shall be used to power SPI BIOS flash on the carrier only.	O 3.3VSB		

Note

1. *The SPI only supports a BIOS flash device by default. The BIOS flash device must be powered from the standby rail. For other options, see section 5.10 "SPI Bus".*

2. *Route the SPI signals as short as possible because of their limited drive strength.*

Table 23 DDI Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
DDI0_PAIR0+ DDI0_PAIR0-	B71 B72	Digital Display Interface 0 Pair 0 differential pairs	O DP		
DDI0_PAIR1+ DDI0_PAIR1-	B73 B74	Digital Display Interface 0 Pair 1 differential pairs	O DP		
DDI0_PAIR2+ DDI0_PAIR2-	B75 B76	Digital Display Interface 0 Pair 2 differential pairs	O DP		
DDI0_PAIR3+ DDI0_PAIR3-	B81 B82	Digital Display Interface 0 Pair 3 differential pairs	O DP		
DDI0_HPD	B89	Digital Display Interface Hot Plug Detect	I 3.3V	PD 1M	
DDI0_CTRLCLK_AUX+	B98	DP AUX+ function if DDI1_DDC_AUX_SEL is no connect.	I/O	PD 100k	
		I2C CTRLCLK if DDI1_DDC_AUX_SEL is pulled high	I/O OD 3.3V	PD 100k	
DDI0_CTRLDATA_AUX-	B99	DP AUX- function if DDI1_DDC_AUX_SEL is no connect.	I/O	PU 100k 3.3V	
		I2C CTRLDATA if DDI1_DDC_AUX_SEL is pulled high.	I/O OD 3.3V	PU 100k 3.3V	
DDI0_DDC_AUX_SEL	B95	Selects the function of DDI0_CTRLCLK_AUX+ and DDI0_CTRLDATA_AUX-.	I 3.3V	PD 1M	

Table 24 DP++ Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
DP0_LANE0+ DP0_LANE0-	B71 B72	Uni-directional main link for the transport of isochronous streams and secondary data.	O DP		
DP0_LANE1+ DP0_LANE1-	B73 B74	Uni-directional main link for the transport of isochronous streams and secondary data.	O DP		
DP0_LANE2+ DP0_LANE2-	B75 B76	Uni-directional main link for the transport of isochronous streams and secondary data..	O DP		
DP0_LANE3+ DP0_LANE3-	B81 B82	Uni-directional main link for the transport of isochronous streams and secondary data.	O DP		
DP0_HPD	B89	Detection of Hot Plug / Unplug and notification of the link layer.	I 3.3V	PD 1M	
DP0_AUX+	B98	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O	PD 100k	
DP0_AUX-	B99	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access.	I/O	PU 100k 3.3V	

Table 25 General Purpose Serial Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SER0_TX	A98	General purpose serial port transmitter.	O 3.3V	3.3V	12 volt tolerant
SER0_RX	A99	General purpose serial port receiver.	I 3.3V	PU 47K 3.3V	12 volt tolerant
SER1_TX / CAN_TX	A101	General purpose serial port transmitter (default). TX output for CAN Bus can be enabled via BIOS Setup menu.	O 3.3V	3.3V	12 volt tolerant
SER1_RX / CAN_RX	A102	General purpose serial port receiver (default). RX input for CAN Bus can be enabled via BIOS Setup menu.	I 3.3V	PU 47K 3.3V	12 volt tolerant

Note

The SER1 options are described in section 5.8 "UART/CAN".

For the correct implementation, see the COM Express® Design Guide.

Table 26 I2C Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
I2C_CK	B33	General purpose I2C port clock output	I/O OD 3.3VSB	PU 2.2K 3.3VSB	
I2C_DAT	B34	General purpose I2C port data I/O line	I/O OD 3.3VSB	PU 2.2K 3.3VSB	

Table 27 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPKR	B32	Output for audio enunciator, the "speaker" in PC-AT systems	O 3.3V		
WDT	B27	Output indicating that a watchdog time-out event has occurred.	O 3.3V	PD 100K	
FAN_PWMOUT	B101	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	O 3.3V	PU 10K 3.3V	12V tolerant
FAN_TACHIN	B102	Fan tachometer input.	I	PU 10K 3.3V	Requires a fan with a two pulse output. 12V tolerant.
TPM_PP	A96	Physical Presence pin of Trusted Platform Module (TPM). Active high.	I 3.3V	PD 10K	not connected (onboard TPM 2.0 does not use it)

Note

For the correct fan control (FAN_PWMOUT, FAN_TACHIN) implementation, see the COM Express® Design Guide.

Table 28 Power and System Management Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PWRBTN#	B12	Power button to bring system out of S5 (soft off), active on falling edge.	I 3.3VSB	PU 20k 3.3VSB	
SYS_RESET#	B49	Reset button input. Active low input. Edge triggered. System will not be held in hardware reset while this input is kept low.	I 3.3VSB	PU 10K 3.3VSB	
CB_RESET#	B50	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a main power input (VIN) that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.	O 3.3VSB	PD 100k	
PWR_OK	B24	Power OK from main power supply. A high value indicates that the power is good.	I 3.3V	PU 10k	
SUS_STAT# / ESPI_RESET#	B18	Indicates the system will enter a low power state soon. Used to notify LPC devices. Reset eSPI interface for both master and slaves. Typically driven from eSPI master to eSPI slaves.	O 3.3VSB O 1.8V	PD 75k	SUS_STAT# (default) Assembly option: eSPI
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board may be used to enable the non-standby power on a typical ATX power supply.	O 3.3VSB	PD 100k	
SUS_S4#	A18	Indicates system is in Suspend to Disk (S4) or Soft Off (S5) state. Active low output.	O 3.3VSB	PD 100k	
SUS_S5#	A24	Indicates system is in Soft Off state.	O 3.3VSB	PD 100k	
WAKE0#	B66	PCI Express wake up request signal.	I 3.3VSB	PU 10k 3.3VSB	
WAKE1#	B67	General purpose wake up signal. May be used to implement a wake-up request from an external device.	I 3.3VSB	PU 10k 3.3VSB	
BATLOW#	A27	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low.	I 3.3VSB	PU 10k 3.3VSB	
LID#	A103	Lid button. Used by the ACPI operating system for a LID switch.	I 3.3VSB	PU 10k 3.3VSB	
SLEEP#	B103	Sleep button. Used by the ACPI operating system to bring the system to sleep state or to wake it up again.	I 3.3VSB	PU 10k 3.3VSB	

Table 29 Thermal Protection Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
THRM#	B35	Input from off-module temp sensor indicating an over temperature situation	I 3.3V	PU 10k 3.3V	
THRMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown	O 3.3V		

Table 30 SM Bus Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SMB_CK	B13	System Management Bus bidirectional clock line	I/O OD 3.3VSB	PU 2k2 3.3VSB	
SMB_DAT	B14	System Management Bus bidirectional data line	I/O OD 3.3VSB	PU 2k2 3.3VSB	
SMB_ALERT#	B15	System Management Bus Alert - Active low input can be used to generate an SMI# (System Management Interrupt)	I 3.3VSB	PU 10k 3.3VSB	

Note

The SMBus options are described in section 5.12 "SMBus".

Table 31 General Purpose I/O Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GPI0	A54	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA0. Bidirectional signal	I 3.3VSB	PU 10K 3.3V	
GPI1	A63	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA1. Bidirectional signal	I 3.3VSB	PU 10K 3.3V	
GPI2	A67	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA2. Bidirectional signal	I 3.3VSB	PU 10K 3.3V	
GPI3	A85	General purpose input pins. Pulled high internally on the module. Shared with SD_DATA3. Bidirectional signal.	I 3.3VSB	PU 10K 3.3V	
GPO0	A93	General purpose output pins. Shared with SD_CLK. Output from COM Express, input to SD	O 3.3VSB		
GPO1	B54	General purpose output pins. Shared with SD_CMD. Output from COM Express, input to SD	O 3.3VSB		
GPO2	B57	General purpose output pins. Shared with SD_WP. Output from COM Express, input to SD	O 3.3VSB		
GPO3	B63	General purpose output pins. Shared with SD_CD#. Output from COM Express, input to SD	O 3.3VSB		

Table 32 SDIO Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SDIO_CD#	B63	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present. Maps to GPO3; used as an input when used for SD card support	I 3.3V	PU 10k	
SDIO_CLK	A93	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs. This signal has maximum frequency of 48 MHz. Maps to GPO0.	O 3.3V		
SDIO_CMD	B54	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode. Maps to GPO1	O 3.3V		
SDIO_WP	B57	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards. Maps to GPO2; used as an input when used for SD card support	I 3.3V	PU 10k	
SDIO_DAT0	A54	SDIO Data line. Operates in push-pull mode and maps to GPI0	IO 3.3V		
SDIO_DAT1	A63	SDIO Data line. Operates in push-pull mode and maps to GPI1	IO 3.3V		
SDIO_DAT2	A67	SDIO Data line. Operates in push-pull mode and maps to GPI2	IO 3.3V		
SDIO_DAT3	A85	SDIO Data line. Operates in push-pull mode and maps to GPI3	IO 3.3V		

Table 33 Module Type Definition Signal Description

Signal	Pin #	Description	I/O	PU/PD	Comment
TYPE10#	A97	Indicates to the carrier board that a Type 10 module is installed.	PDS	PD 47k	

Table 34 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	A104-A109 B104-B109	Primary power input: 4.75V to 20V. All available VCC_12V pins on the connector(s) shall be used.	P		The conga-MA7 is a Type 10 mini module and as such supports a wide power supply range between 4.75 and 20V.
VCC_5V_SBY	B84-B87	Standby power input: +5V nominal. If VCC5V_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. May be left unconnected if these functions are not used in the system design.	P		
VCC_RTC	A47	Real time clock circuit-power input: +3V nominal	P		
GND	A1, A11, A21, A31, A41, A51, A57, A60, A66, A70, A80, A90, A100, A110 B1, B11, B21, B31, B41, B51, B60, B70, B80, B90, B100, B110	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to carrier board GND plane.	P		

9 System Resources

9.1 I/O Address Assignment

The I/O address assignment of the conga-MA7 module is functionally identical with a standard PC/AT. The table below shows the most important addresses and the addresses that differ from the standard PC/AT configuration.

These Fixed address ranges are either positively decoded in the System Agent or subtractively routed to the Primary to Sideband Bridge (P2SB). The P2SB will claim many of the fixed I/O accesses and forward those transactions over sideband fabric to their functional target. Address ranges that are not listed or marked Reserved are NOT positively decoded by the PCH (unless assigned to one of the variable ranges) and will be internally terminated by the PCH.

On the conga-MA7 the Platform P2SB acts as the subtractive decoding agent. I/O Fix Addresses positively decoded by system Agents are listed in the following table.

Table 35 I/O Address Assignment

Device	I/O Address (hex)
Interrupt Controller	20h-21h, 24h-25h, 28h-29h, 2Ch-2Dh, 30h-31h, 34h-35h, 38h-39h, 3Ch-3Dh, A0h- A1h, A4h-A5h, A8h-A9h, ACh-ADh, B0h-B1h, B4h-B5h, B8h-B9h, Bch-BDh, 4D0h-4D1h
8254 Timers	40h-43h, 50h-53h
NMI Controller (CPU I/F)	61h, 63h, 65h, 67h
Reset Generator (CPU I/F)	92h
RTC	70h-77h
Reset Generator (CPU)	CF9h
PMC	B2h-B3h
eSPI	2Eh-2F, 4Eh-4Fh, 60h, 62h, 64h, 66h, 80h, 84h-86h, 8Ch-8Eh, 90h, 94h-96h, 98h, 9Ch-9Eh, 200-207h, 208-20Fh, 2F8-2FFh, 3F8-3FFh, E00h-EFFh

The LPC interface is connected to the Enhanced Serial Peripheral Interface (eSPI) controller of the SoC via a Microchip ECE1200 eSPI to LPC bridge (Secondary Slave) by default.

9.2 PCI Configuration Space Map

Bus Number	Device Number	Function Number	Device ID	Description
00h	00h	00h	0x452E	Host Bridge
00h	02h	00h	0x4571	Graphics and Display
00h	12h	00h	0x4B37	Intel® Serial I/O: SPI Controller #2
00h	14h	00h	0x4B7D	USB eXtensible Host Controller Interface (xHCI)
00h	14h	01h	0x4B7E	USB eXtensible Device Controller Interface (xDCI) [2]
00h	14h	02h	0x4B7F	Memory Controller
00h	16h	00h	0x4B70	Intel® Converged Security Engine (Intel® CSE)
00h	17h	00h	0x4B63	SATA Controller (AHCI)
00h	18h	00h	0x4BC0	Intel® Programmable Services Engine (Intel® PSE): I2C Controller #7
00h	18h	01h	0x4BC1	Intel® PSE: CAN Controller #0 [2]
00h	1Ah	00h	0x4B47	embedded Multi Media Card (eMMC) Controller
00h	1Ah	01h	0x4B48	Secure Digital (SD) & Secure Digital I/O Controller
00h	1Bh	00h	0x4BB9	Intel® PSE: Inter-Integrated Circuit (I2C) Controller #0
00h	1Ch	00h	0x4B38	PCIe Root Port #0 (PCIe 0, Single VC) [1]
00h	1Ch	01h	0x4B39	PCIe Root Port #1 (PCIe 0, Single VC) [1]
00h	1Ch	02h	0x4B3A	PCIe Root Port #2 (PCIe 0, Single VC) [1]
00h	1Ch	03h	0x4B3B	PCIe Root Port #3 (PCIe 0, Single VC) [1]
00h	1Ch	04h	0x4B3C	PCIe Root Port #4 (PCIe 1, Multi VC) [1]
00h	1Ch	05h	0x4B3D	PCIe Root Port #5 (PCIe 2, Multi VC) [1]
00h	1Ch	06h	0x4B3E	PCIe Root Port #6 (PCIe 3, Multi VC) [1]
00h	1Dh	00h	0x4BB3	Intel® Programmable Services Engine (Intel® PSE): Local Host to PSE (LH2OSE) IPC
00h	1Dh	01h	0x4BA0	Intel® PSE: Gigabit Ethernet Time Sensitive Networking (TSN) Controller #0 (RGMII: 1Gb Mode)
00h	1Dh	02h	0x4BB0	Intel® PSE: Gigabit Ethernet Time Sensitive Networking (TSN) Controller #1 (RGMII: 1Gb Mode)
00h	1Eh	00h	0x4B28	Intel® Serial I/O: UART Controller #0 [2]
00h	1Fh	00h	0x4B00	Enhanced Serial Peripheral Interface (eSPI) Controller
00h	1Fh	01h	0x4B20	Primary to Sideband Bridge (P2SB)
00h	1Fh	02h	0x4B21	Power Management Controller (PMC)
00h	1Fh	04h	0x4B23	System Management Bus (SMBus) Controller
00h	1Fh	05h	0x4B24	Serial Peripheral Interface (SPI) Controller for Flash & TPM
00h	1Fh	07h	0x4B26	Intel® Trace Hub

Note

1. *To view these ports, attach a device to the corresponding PCI Express port or set the PCI Express port in the BIOS setup menu to "Enabled".*
2. *Disabled by default in the BIOS Setup menu.*

9.3 I²C Bus

There are no onboard resources connected to the I²C bus. Address 16h is reserved for congatec Battery Management solutions.

9.4 SMBus

System Management (SM) bus signals are connected to the Intel® chipset. The SMBus is not intended to be used by off-board non-system management devices. For more information about this subject, contact congatec technical support.

9.5 congatec System Sensors

conga-MA7 offers several Sensors and Monitors accessible thought CGOS interface and also visible on the Health Monitor Submenu in BIOS Setup.

- 2 Temperature Sensors
  - CPU temperature based on CPU Digital Thermal Sensor
  - Board temperature sensor located on the Board Controller
- 1 Voltage Sensor
  - 5V Standard
- 1 Current Sensor
- 1 Fan Monitor

10 BIOS Setup Description

The BIOS setup description of the conga-MA7 can be viewed without having access to the module. However, access to the restricted area of the congatec website is required in order to download the necessary tool (CgMlfViewer) and Menu Layout File (MLF).

The MLF contains the BIOS setup description of a particular BIOS revision. The MLF can be viewed with the CgMlfViewer tool. This tool offers a search function to quickly check for supported BIOS features. It also shows where each feature can be found in the BIOS setup menu.

For more information, read the application note "AN42 - BIOS Setup Description" available at www.congatec.com.

Note

If you do not have access to the restricted area of the congatec website, contact your local congatec sales representative.

10.1 Navigating the BIOS Setup Menu

The BIOS setup menu shows the features and options supported in the congatec BIOS. To access and navigate the BIOS setup menu, press the <DEL> or <F2> key during POST.

The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

10.2 BIOS Versions

The BIOS displays the BIOS project name and the revision code during POST, and on the main setup screen. The initial production BIOS for conga-MA7 is identified as MA70R1xx, where:

- MA7 is the project name
- R is the identifier for a BIOS ROM file
- 1 is the feature number
- xx is the major and minor revision number.

The binary size of conga-MA7 BIOS is 32 MByte.

10.3 Updating the BIOS

BIOS updates are recommended to correct platform issues or enhance the feature set of the module. The conga-MA7 features a congatec/AMI AptioEFI firmware on an onboard flash ROM chip. You can update the firmware with the congatec System Utility. The utility has five versions—UEFI shell, DOS based command line[1], Win32 command line, Win32 GUI, and Linux version.

For more information about "Updating the BIOS" refer to the user's guide for the congatec System Utility "CGUTLm1x.pdf" on the congatec website at www.congatec.com.

Note

1. *Deprecated*

Caution

The DOS command line tool is not officially supported by congatec and therefore not recommended for critical tasks such as firmware updates. We recommend to use only the UEFI shell for critical updates.

10.4 Supported Flash Devices

The conga-MA7 supports the following flash device:

- Macronix MX25L25645G (32MB)

The flash devices listed above can be used on the carrier board for external BIOS support. For more information about external BIOS support, refer to the Application Note "AN7_External_BIOS_Update.pdf" on the congatec website at www.congatec.com.