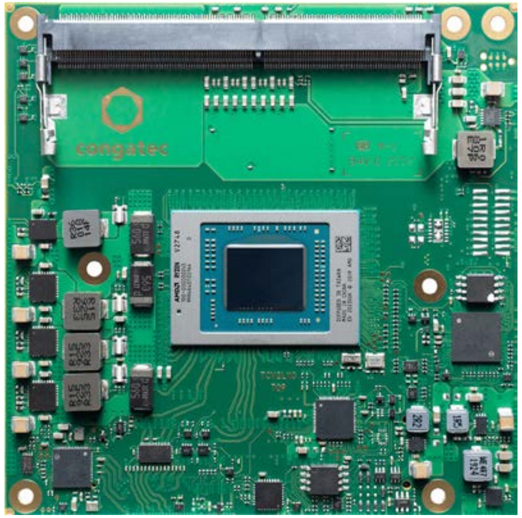

conga-TCV2

COM Express® 3.0 Type 6 Compact Module with AMD Ryzen Embedded V2000 Processors

User's Guide

Revision 1.02

Revision History

Revision	Date (yyyy-mm-dd)	Author	Changes
0.1	2021-11-22	AEM	• Preliminary release
1.00	2022-11-14	AEM	• Corrected the TDP range of AMD Ryzen™ Embedded V2718 and V2716 in section 1.2 "Options Information" • Added linformation about the conga-TCV2 Errata in section 2.1 "Feature List" • Added note about native UEFI Operating System in section 2.2 "Supported Operating Systems" • Updated table 6 "Power Consumption Values" and table 7 "CMOS Battery Power Consumption" • Updated table 35 "General Purpose Serial Interface Signal Descriptions" • Updated section 3 "Block Diagram" • Updated sections 5.1.1 "PCI Express", added table 11 "COM Express PCIe Configuration" to section 5.1.1 "PCI Express" and updated section 5.1.2 "PCI Express Graphics (PEG)) • Deleted section 6.3.4 "OEM BIOS Code/Data" • Added section 9 "System Resources" • Official release
1.01	2023-12-12	AEM	• Updated the title page • Updated the RoHS statement • Added a note about optimal storage conditions to section 2.7 "Environmental Specifications" • Added note about the storage of congatec cooling solutions to section 4 "Cooling Solutions" • Updated section 6.2 "congatec Board Controller (cBC)" • Updated section 6.2.3 "Power Loss Control" • Updated section 6.2.5 "Enhanced Soft-Off State" • Updated the note in table 35 "General Purpose Serial Interface Signal Descriptions" • Added note to table 29 "Miscellaneous Signal Descriptions" • Added note to table 31 "Power and System Management Signal Descriptions"
1.02	2024-11-08	AEM	• Corrected the revision of the COM Express® specification on the title page and in section 1.1 "COM Express® Concept" • Deleted duplicated sentence in section 1.1 "COM Express® Concept" • Added note for MAC address programming to section 5.1.6 "Gigabit Ethernet" and table 25 "Gigabit Ethernet Signal Descriptions" • Added a caution to table 14 "Connector C-D Pinout"

Preface

This user's guide provides information about the components, features and interfaces available on the conga-TCV2. It is one of three documents that should be referred to when designing a COM Express® application. The other reference documents that should be used include the following:

- COM Express® Module Base Specification
- COM Express® Carrier Design Guide

These documents are available on the PICMG website at **www.picmg.org**. Additionally, check the restricted area of the congatec website at **www.congatec.com** and the website of the respective silicon vendor for relevant documents (Erratum, PCN, Sighting Reports and others).

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The following symbols are used in this user’s guide:

Warning

Warnings indicate conditions that, if not observed, can cause personal injury.

Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.

Note

Notes call attention to important information that should be observed.

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Terminology

Term	Description
CSA	Active Cooling Solution
CSP	Passive Cooling Solution
cBC	congatec Board Controller
COM	Computer-on-Module
DDI	Digital Display Interface
DTR	Dynamic Temperature Range
GB	Gigabyte
Gbe	Gigabit Ethernet
HDA	High Definition Audio
HSP	Heatspreader
LVDS	Low-Voltage Differential Signaling
MB	Megabyte
MHz	Megahertz
MT/s	Megatransfers per second
N.A.	Not available
N.C.	Not connected
PCIe	PCI Express
PWM	Pulse Width Modulation
RTS	Real Time Systems
SoC	System On Chip
TBD	To be determined
TDP	Thermal Design Power
UART	Universal Asynchronous Receiver/Transmitter

Contents

List of Tables

1 Introduction

1.1 COM Expres® Concept

COM Express® is an open industry standard defined specifically for COMs (computer on modules). Its creation makes it possible to smoothly transition from legacy interfaces to the newest technologies available today. COM Express® modules are available in following form factors:

Mini	84 mm x 55 mm
Compact	95 mm x 95 mm
Basic	125 mm x 95 mm
Extended	155 mm x 110 mm

Table 1 COM Express® 3.0 Pinout Types

Types	Connector Rows	PCIe Lanes	PEG	SATA Ports	LAN ports	USB 2.0/ SuperSpeed USB	Display Interfaces
Type 6	A-B C-D	Up to 24	1	Up to 4	1	Up to 8 / 4 [1]	VGA,LVDS/eDP, PEG, 3x DDI
Type 7	A-B C-D	Up to 32	-	Up to 2	5 (1x 1 Gb, 4x 10 Gb)	Up to 4 / 4	
Type 10	A-B	Up to 4	-	Up to 2	1	Up to 8 / 2 [1]	LVDS/eDP, 1xDDI

[1] *The SuperSpeed USB ports are not in addition to the USB 2.0 ports. Up to four of the USB 2.0 ports can support SuperSpeed USB.*

The conga-TCV2 modules use the Type 6 pinout definition and comply with COM Express® 3.0 specification. They are equipped with two high performance connectors that ensure stable data throughput.

The COM integrates all the core components and is mounted onto an application specific carrier board. COM modules are legacy-free design (no Super I/O, PS/2 keyboard and mouse) and provide most of the functional requirements for any application. These functions include, but are not limited to a rich complement of contemporary high bandwidth serial interfaces such as PCI Express, Serial ATA, USB 2.0, and Gigabit Ethernet. The robust thermal and mechanical concept, combined with extended power-management capabilities, is perfectly suited for all applications.

Carrier board designers can use as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration.

Most importantly, COM Express® modules are scalable, which means once an application has been created there is the ability to diversify the product range through the use of different performance class or form factor size modules. Simply unplug one module and replace it with another; no redesign is necessary.

1.2 Options Information

The conga-TCV2 is currently available in four variants. The table below shows the different configurations available.

Table 2 conga-TCV2 Variants

Part-No.	050500	050501	050502	050503
Processor	AMD Ryzen™ Embedded V2748, 2.9 GHz, 8 Core	AMD Ryzen™ Embedded V2546, 3.0 GHz, 6 Core	AMD Ryzen™ Embedded V2718, 1.7 GHz, 8 Core	AMD Ryzen™ Embedded V2516, 2.1 GHz, 6 Core
CPU Max Freq.	4.25 GHz	3.95 GHz	4.15 GHz	3.95 GHz
L2/L3 Shared Cache	4 MB/8 MB	3 MB/8 MB	4 MB/8 MB	3 MB/8 MB
DDR4 Memory (ECC or Non-ECC)	3200 MT/s dual channel	3200 MT/s dual channel	3200 MT/s dual channel	3200 MT/s dual channel
Graphics Engine	AMD Radeon™ (7 Compute Units)	AMD Radeon™ (6 Compute Units)	AMD Radeon™ (7 Compute Units)	AMD Radeon™ (6 Compute Units)
Graphics Freq.	1.6 GHz	1.5 GHz	1.6 GHz	1.5 GHz
PCIe Ports (Lanes)	5x PCIe Gen 3 Ports (8 lanes)	5x PCIe Gen 3 Ports (8 lanes)	5x PCIe Gen 3 Ports (8 lanes)	5x PCIe Gen 3 Ports (8 lanes)
USB	4x USB 3.1 Gen 2 4x USB 2.0	4x USB 3.1 Gen 2 4x USB 2.0	4x USB 3.1 Gen 2 4x USB 2.0	4x USB 3.1 Gen 2 4x USB 2.0
SATA (6 Gb/s)	2x5	2x	2x	2x
DDI	3x DP++	3x DP++	3x DP++	3x DP++
LVDS/eDP	Single or dual LVDS	Single or dual LVDS	Single or dual LVDS	Single or dual LVDS
SoC TDP	45 W (35 W – 54 W)	45 W (35 W – 54 W)	15 W (10 W – 25 W)	15 W (10 W – 25 W)

2 Specifications

2.1 Feature List

Table 3 Feature Summary

Form Factor	Based on COM Express® standard pinout Type 6 (Compact size 95 x 95 mm)	
SoC	AMD Ryzen™ Embedded V2000	
Memory	Two memory sockets (located on the top and bottom side of the conga-TCV2). Supports: - SO-DIMM ECC/non-ECC DDR4 memory modules - Data rates up to 3200 MT/s - Maximum 64 GB capacity (32 GB on each socket)	
Chipset	Integrated in the SoC	
Audio	High Definition Audio (HDA) interface	
Ethernet	2.5 Gigabit Ethernet controller (Intel i225V)	
Graphics Options	AMD Radeon™ Graphics supports: - API (DirectX® 12, EGL 1.4, OpenCL® 2.1, OpenGL® ES (1.1, 2.x and 3.x), OpenGL® Next, OpenGL® 4.6) - Multimedia hardware accelerator supporting H.264/AVC (8-bit) encode and decode, H.265/HEVC (8-bit and 10-bit) encode and decode, VP9 (8-bit and 10-bit) decode, MS compliant JPEG encode and decode - Up to four independent displays (see table 10 "Display Combinations and Resolution")	
	3x DP++ 1x LVDS/eDP 1.3 PEG x8 port Resolutions up to 4K @ 60 Hz	**NOTE**: *The conga-TCV2 does not natively support TMDS. A DP++ to TMDS converter (e.g. PTN3360D) needs to be implemented on the carrier board.*
Peripheral Interfaces	4x USB 3.1 Gen 2	GPIOs
	4x USB 2.0	LPC
	2x SATA® (6 Gbps)	I²C (fast mode, multi-master)
	5x PCIe (8 Gen. 3 lanes)	SMB
	2x UART (16C550 compatible)	SPI
BIOS	AMI Aptio® V UEFI 2.x firmware 32 MB serial SPI flash with congatec Embedded BIOS features	
Power Management	ACPI 5.0 compliant with battery support. S5e mode (see section 6.2.5 "Enhanced Soft-Off State") Suspend to RAM (S3)	
cBC	Multi-stage watchdog, non-volatile user data storage, manufacturing and board information, board statistics, hardware monitoring, fan control, I2C bus, Power loss control	
Security	Discrete SPI TPM (Infineon SLB9670VQ2.0); AES Instructions	

Note

For conga-TCV2 Errata, log in to the restricted area of the congatec website and go to the Technical Information -> Technical Documents (Fact Sheet, Erratum) section.

2.2 Supported Operating Systems

The conga-TCV2 supports the following operating systems.

- Microsoft® Windows® 10 (64-bit)
- Microsoft® Windows® 10 IoT Enterprise (64-bit)
- Linux LTS (64-bit)
- Real-Time Systems Hypervisor

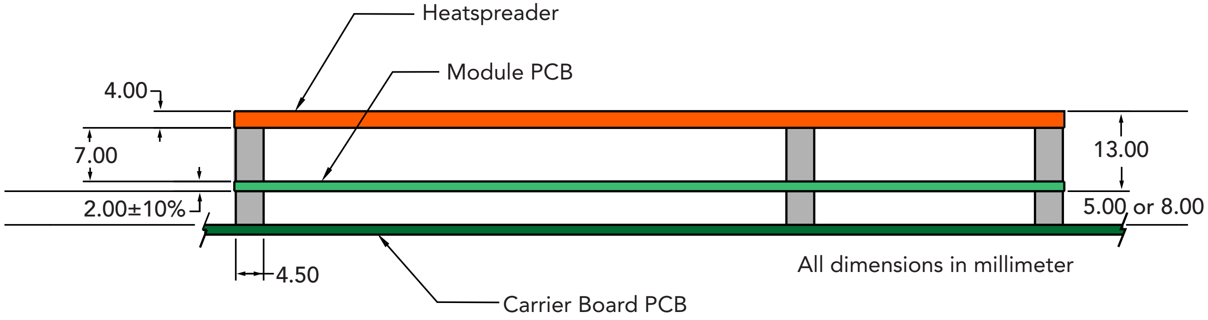
Note

1. *Install AMD catalyst driver after installing Microsoft® Windows® Operating System to improve the graphic performance of the conga-TCV2.*
2. *The conga-TCV2 supports only native UEFI Operating Systems. Legacy Operating Systems which require CSM (Compatibility Suppport Module) as part of the UEFI firmware are not supported anymore.*

2.3 Mechanical Dimensions

- Length of 95 mm
- Width of 95 mm
- Height of 11 mm (5 mm top-side, 2 mm PCB and 4 mm bottom-side)

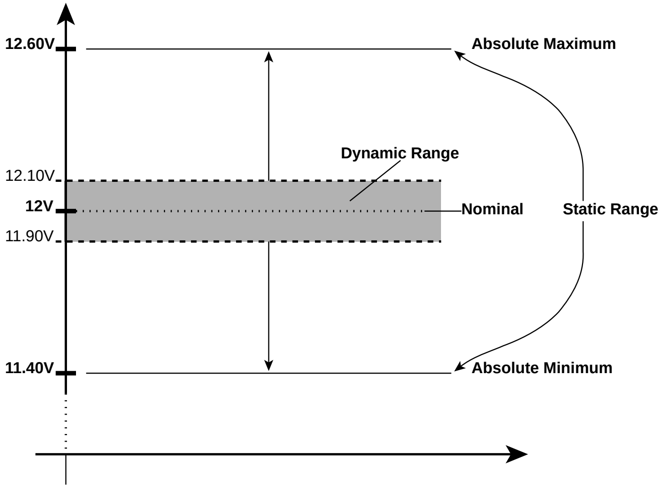
The overall height for heatspreader is shown below:



2.4 Supply Voltage Standard Power

- 12 V DC ± 5%

The dynamic range shall not exceed the static range.



2.4.1 Electrical Characteristics

Power supply pins on the module's connectors limit the amount of input power. The following table provides an overview of the limitations for pinout Type 6 (dual connector, 440 pins).

Table 4 Electrical Characteristics

Power Rail	Module Pin Current Capability (Ampere)	Nominal Input (Volts)	Input Range (Volts)	Derated Input (Volts)	Max. Input Ripple (10Hz to 20MHz) (mV)	Max. Module Input Power (w. derated input) (Watts)	Assumed Conversion Efficiency	Max. Load Power (Watts)
VCC_12V	12	12	11.4-12.6	11.4	+/- 100	137	85%	116
VCC_5V-SBY	2	5	4.75-5.25	4.75	+/- 50	9		
VCC_RTC	0.5	3	2.5-3.3		+/- 20			

2.4.2 Rise Time

The input voltages shall rise from 10% of nominal to 90% of nominal at a minimum slope of 250V/s. The smooth turn-on requires that during the 10% to 90% portion of the rise time, the slope of the turn-on waveform must be positive.

2.5 Power Consumption

The power consumption values were measured with the following setup:

- conga-TCV2 module
- modified congatec carrier board
- conga-TCV2 cooling solution
- Microsoft Windows® 10 (64-bit)

Note

The SoC was stressed to its maximum workload with the AMD Validation Toolkit (AVT).

Table 5 Measurement Description

The power consumption values were recorded during the following system states:

System State	Description	Comment
S0: Minimum value	Lowest frequency mode (LFM) with minimum core voltage during desktop idle	
S0: Maximum value	Highest frequency mode (HFM/Turbo Boost)	The CPU was stressed to its maximum frequency
S0: Peak current	Highest current spike during the measurement of "S0: Maximum value". This state shows the peak value during runtime.	Consider this value when designing the system's power supply to ensure that sufficient power is supplied during worst case scenarios
S3	COM is powered by VCC_5V_SBY	
S5	COM is powered by VCC_5V_SBY	
S5e	COM is powered by VCC_5V_SBY	

Note

1. *The fan and SATA drives were powered externally.*
2. *All other peripherals except the LCD monitor were disconnected before measurement.*

Table 6 Power Consumption Values

The table below provides additional information about the conga-TCV2 power consumption data. The values were recorded at various operating modes.

Part No.	Memory Size	H.W Rev.	BIOS Rev.	OS (64-bit)	CPU			Current (Ampere)				
					Variant	Cores	Base/ Max Freq. (GHz)	S0: Min	S0: Max	S0: Peak	S3	S5
050500	2 x 8 GB	A.3	TCV2R012	Windows 10	AMD Ryzen™ Embedded V2748	8	2.90 / 4.25	0.22	5.37	6.52	0.11	0.09
050501	2 x 8 GB	A.3	TCV2R012	Windows 10	AMD Ryzen™ Embedded V2546	6	3.00 / 3.95	0.21	6.08	8.84	0.09	0.09
050502	2 x 8 GB	A.3	TCV2R012	Windows 10	AMD Ryzen™ Embedded V2718	8	1.70 / 4.15	0.22	2.75	3.33	0.11	0.09
050503	2 x 8 GB	A.3	TCV2R012	Windows 10	AMD Ryzen™ Embedded V2516	6	2.10 / 3.95	0.23	2.64	3.17	0.11	0.09

Note

With fast input voltage rise time, the inrush current may exceed the measured peak current.

2.6 Supply Voltage Battery Power

Table 7 CMOS Battery Power Consumption

RTC @	Voltage	Current
-10°C	3 V DC	4.59 µA
20°C	3 V DC	3.47 µA
70°C	3 V DC	4.23 µA

Note

1. *Do not use the CMOS battery power consumption values listed above to calculate CMOS battery lifetime.*
2. *Measure the CMOS battery power consumption of your application in worst case conditions (for example, during high temperature and high battery voltage).*
3. *Consider the self-discharge of the battery when calculating the lifetime of the CMOS battery. For more information, refer to application note AN9_RTC_Battery_Lifetime.pdf on congatec GmbH website at www.congatec.com/support/application-notes.*
4. *We recommend to always have a CMOS battery present when operating the conga-TCV2.*

2.7 Environmental Specifications

Temperature (commercial variants)	Operation:	0° to 60°C	Storage: -40° to +85°C
Humidity	Operation:	10% to 90%	Storage: 5% to 95%

Caution

The above operating temperatures must be strictly adhered to at all times. When using a congatec heatspreader, the maximum operating temperature refers to any measurable spot on the heatspreader's surface.

Humidity specifications are for non-condensing conditions.

2.8 Storage Specifications

This section describes the storage conditions that must be observed for optimal performance of congatec products.

2.8.1 Module

For long-term storage of the conga-TCV2 (more than six months), keep the conga-TCV2 in a climate-controlled building at a constant temperature between 5°C and 40°C, with humidity of less than 65% and at an altitude of less than 3000 m. Also ensure the storage location is dry and well ventilated.

Note

We do not recommend storing the conga-TCV2 for more than five years under these conditions.

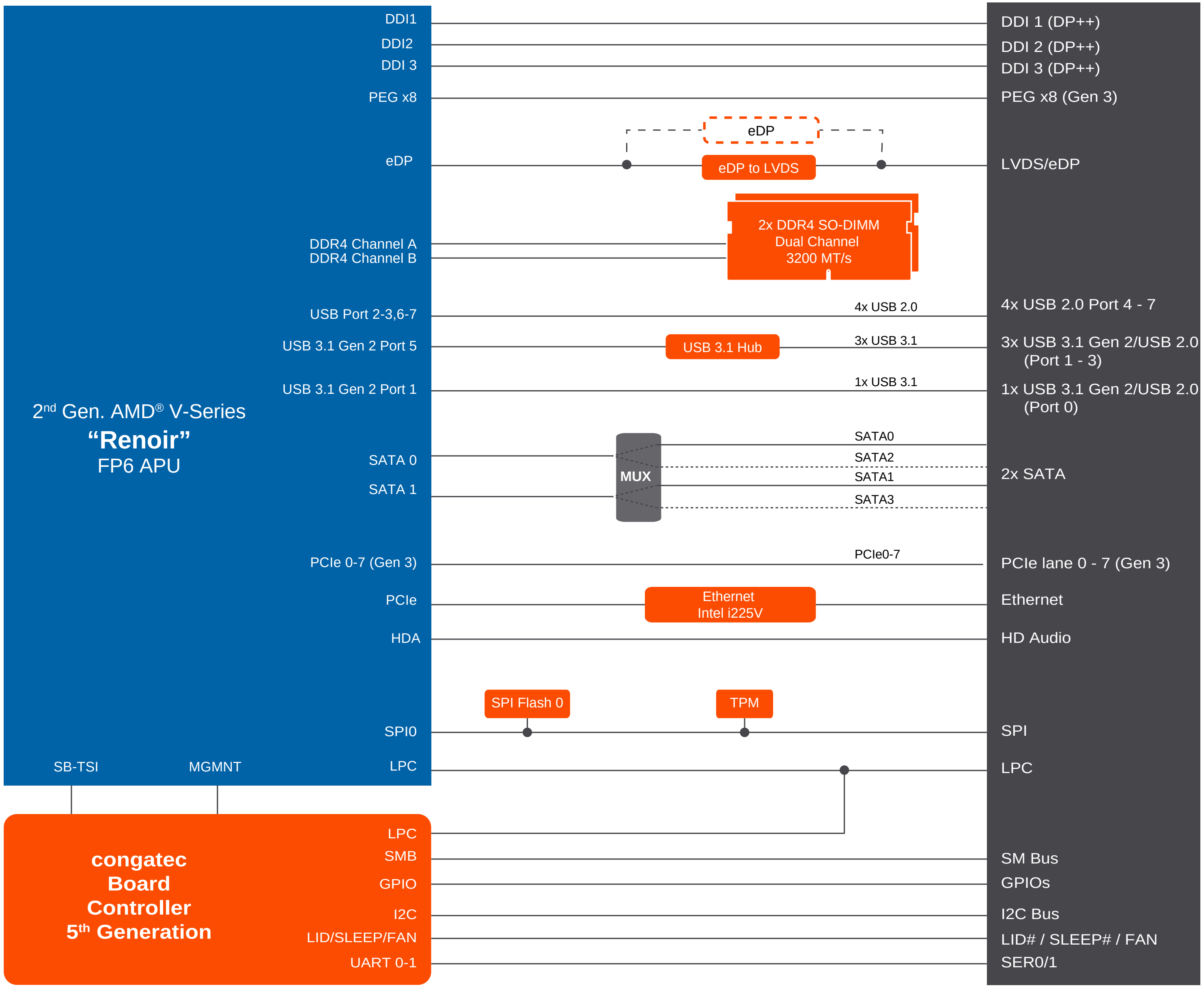
2.8.2 Cooling Solution

The heatpipes of congatec heatspreaders/cooling solutions are filled with water by default. For optimal cooling performance, do not store the heatspreaders/cooling solutions at temperatures below -20°C.

Caution

1. *For temperatures between -10°C and -20°C, preheat the heatpipes before operation. Optionally, the heatpipes can be filled with acetone instead. For more information, contact your local sales representative.*
2. *For optimal thermal dissipation, do not store the congatec cooling solutions for more than six months.*

3 Block Diagram



⁚⁚⁚ Optional - Not available by default

4 Cooling Solutions

congatec GmbH offers the cooling solutions listed in Table 8 for conga-TCV2. The dimensions of the cooling solutions are shown in the sub-sections. All measurements are in millimeters.

Table 8 Cooling Solution Variants

	Cooling Solution	Part No	Description
1	CSA	050550	Active cooling with 2.7 mm bore-hole standoffs.
		050551	Active cooling with M2.5 mm threaded standoffs.
2	CSP	050552	Passive cooling with 2.7 mm bore-hole standoffs.
		050553	Passive cooling with M2.5 mm threaded standoffs.
3	HSP	050554	Heatspreader with 2.7 mm bore-hole standoffs.
		050555	Heatspreader with M2.5 mm threaded standoffs.

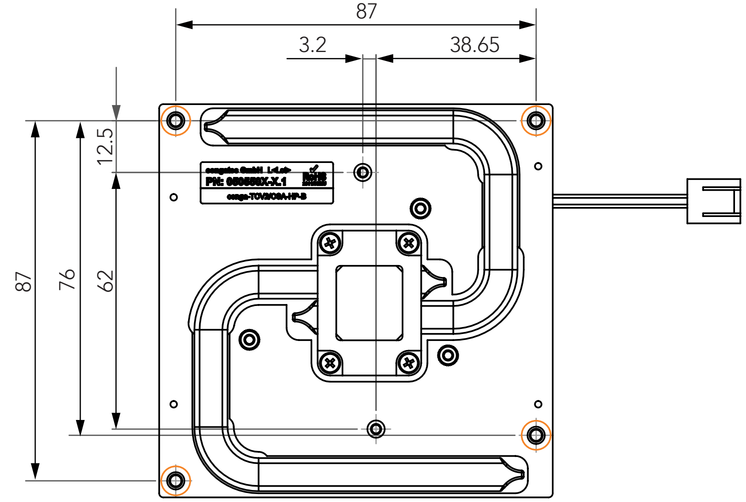
Note

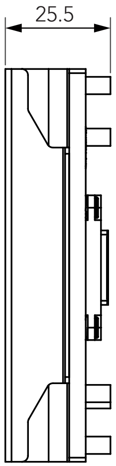
1. *We recommend a maximum torque of 0.4 Nm for carrier board mounting screws and 0.5 Nm for module mounting screws.*
2. *The gap pad material used on congatec heatspreaders may contain silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.*
3. *For optimal thermal dissipation, do not store the congatec cooling solutions for more than six months.*

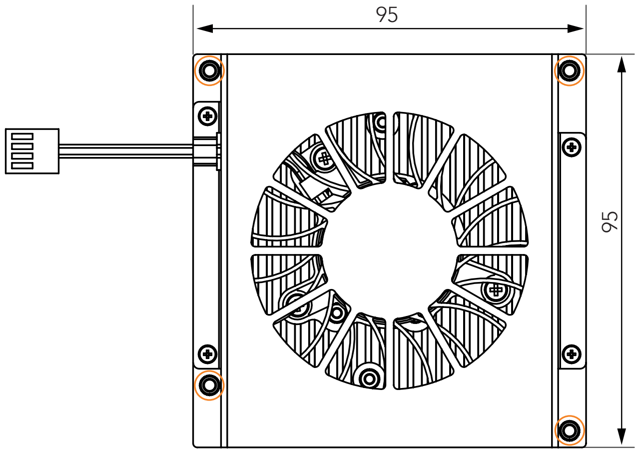
Caution

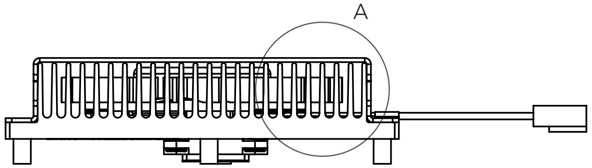
1. *The congatec heatspreaders/cooling solutions are tested only within the commercial temperature range of 0° to 60°C. If your application that features a congatec heatspreader/cooling solution operates outside this temperature range, ensure the correct operating temperature of the module is maintained at all times. This may require additional cooling components for your final application's thermal solution.*
2. *For adequate heat dissipation, use the mounting holes on the cooling solution to attach it to the module. Apply thread-locking fluid on the screws if the cooling solution is used in a high shock and/or vibration environment. To prevent the standoff from stripping or cross-threading, use non-threaded carrier board standoffs to mount threaded cooling solutions.*
3. *For applications that require vertically-mounted cooling solution, use only coolers that secure the thermal stacks with fixing post. Without the fixing post feature, the thermal stacks may move.*
4. *Do not exceed the recommended maximum torque. Doing so may damage the module or the carrier board, or both.*

4.1 CSA Dimensions









M2.5 x 11 mm
threaded standoff
for threaded version
or
ø2.7 x 11 mm
non-threaded standoff
for borehole version

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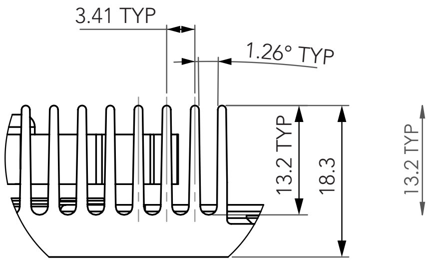
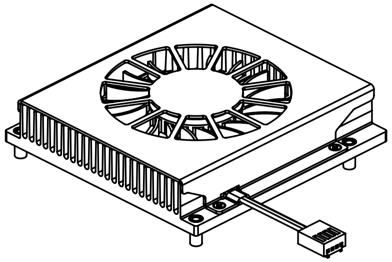
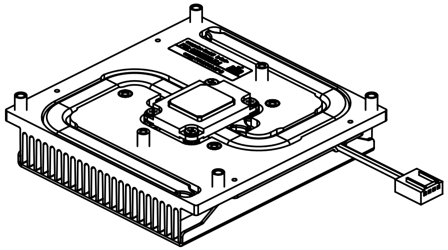
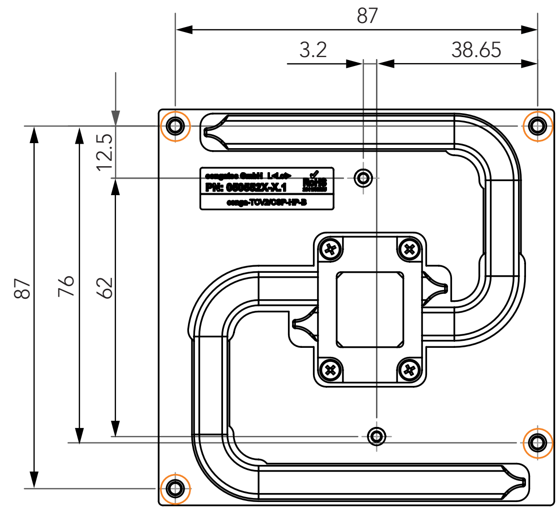
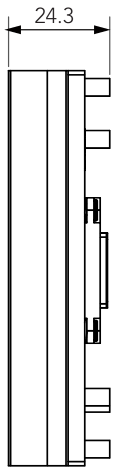


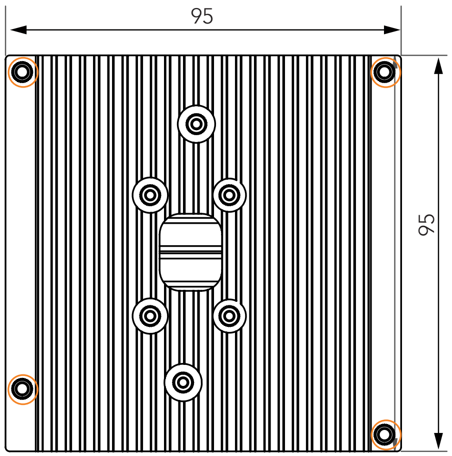


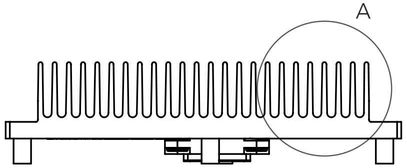


4.2 CSP Dimensions



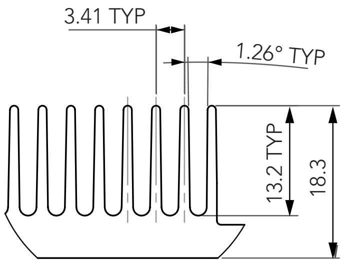


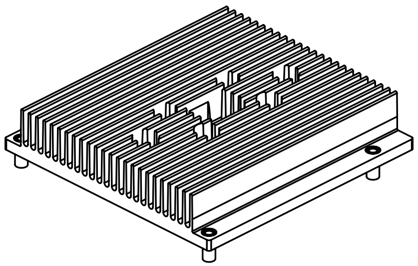


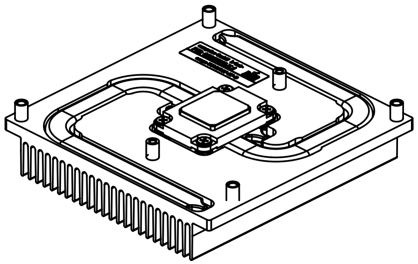


◎ M2.5 x 11 mm threaded standoff for threaded version or ø2.7 x 11 mm non-threaded standoff for borehole version

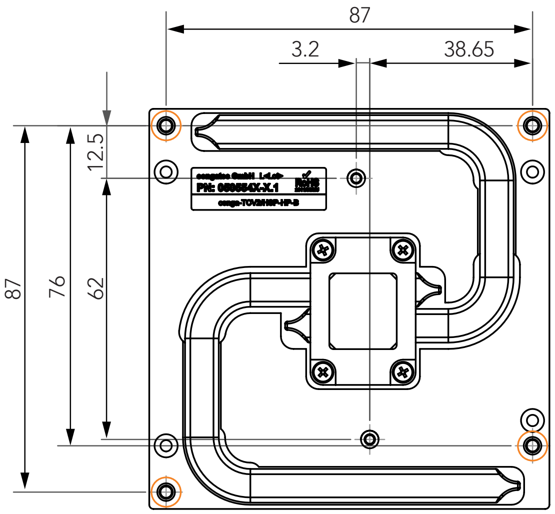
A (2 : 1)

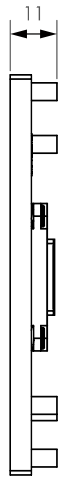


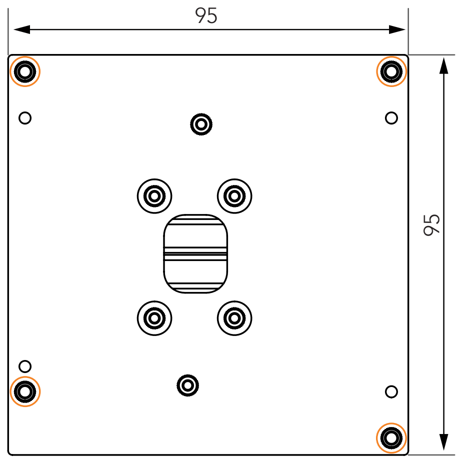


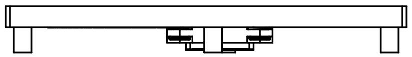


Heatspreader Dimensions

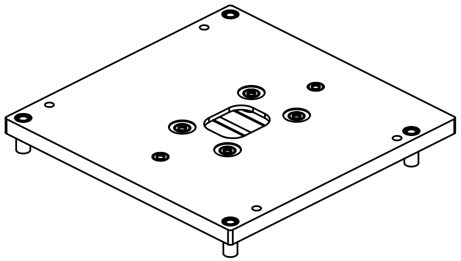


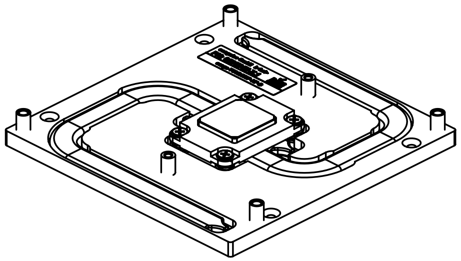






M2.5 x 11 mm
threaded standoff
for threaded version
or
ø2.7 x 11 mm
non-threaded standoff
for borehole version





5 Connector Rows

The conga-TCV2 is connected to the carrier board via two 220-pin connectors (COM Express® Type 6 pinout). These connectors are broken down into four rows. The primary connector consists of rows A and B while the secondary connector consists of rows C and D.

5.1 Primary and Secondary Connector Rows

The following subsystems can be found on the primary connector rows A and B.

5.1.1 PCI Express™

The conga-TCV2 offers five PCIe ports with eight PCIe lanes—six on the A–B connector and two on the C–D connector. The lanes support:

- up to 8 GT/s (Gen 3) speed
- a 1 x4 + 4 x1 default link configuration
- a 2 x4 link, 2 x2 + 1 x4 link or 2 x1 + 1 x2 + 1 x4 link via the BIOS setup menu
- lane polarity inversion

Table 9 COM Express® PCIe Configuration

Options	Configurations							
	PCIe0	PCIe1	PCIe2	PCIe3	PCIe4	PCIe5	PCIe6	PCIe7
Default	x4				x1	x1	x1	x1
BIOS Setup Menu	x4				x4			
BIOS Setup Menu	x2		x2		x4			
BIOS Setup Menu	x2		x1	x1	x4			
BIOS Setup Menu	x1	x1	x2		x4			
BIOS Setup Menu	x1	x1	x1	x1	x4			

5.1.2 PCI Express™ Graphics (PEG)

The conga-TCV2 offers a x8 Gen 3 PEG port on the C–D connector. The default configuration of the PEG interface is 2 x4 link. The interface can be configured in the BIOS setup menu as a 1 x8 link.

Note

The PEG lanes can not be linked together with the PCI Express lanes in section 5.1.1 "PCI Express™".

5.1.3 Display Interface

The conga-TCV2 supports:

- three DP++ (dual-mode DP)
- single- or dual-channel LVDS
- four independent displays (3x DP++ and 1x LVDS/eDP)

The table below shows the supported display combinations and resolutions.

Table 10 Display Combinations and Resolution

	Display 1 (DDI1)		Display 2 (DDI2)		Display 3 (DDI2)		Display 4	
	Interface	Max. Resolution	Interface	Max. Resolution	Interface	Max. Resolution	Interface	Max. Resolution
Option 1	DP++	4096x2160 @ 60 Hz	DP++	4096x2160 @ 60 Hz	DP++	4096x2160 @ 60 Hz	LVDS	1920x1200 @ 60 Hz (dual LVDS mode)
Option 2	DP++	4096x2160 @ 60 Hz	DP++	4096x2160 @ 60 Hz	DP++	4096x2160 @ 60 Hz	eDP (BOM option)	4096x2160 @ 60 Hz

5.1.3.1 DisplayPort (DP)

The conga-TCV2 supports:

- up to three DP ports
- VESA DisplayPort Standard 1.4
- data rate of 1.62 GT/s, 2.7 GT/s and 5.4 GT/s on 1, 2 or 4 data lanes
- up to 4096x2160 resolutions at 60 Hz
- maximum of three independent DP displays

5.1.3.2 LVDS/eDP

The conga-TCV2 offers an LVDS interface with optional eDP overlay on the A–B connector. The LVDS interface provides LVDS signals by default, but can optionally support eDP signals (assembly option).

The LVDS [1] interface supports:

- single or dual channel LVDS (color depths of 18 bpp or 24 bpp)
- integrated flat panel interface with clock frequency up to 112 MHz

- VESA and OpenLDI LVDS color mappings
- automatic panel detection via Embedded Panel Interface based on VESA EDID™ 1.3
- resolution up to 1920x1200 in dual LVDS channel mode

The eDP [1,2] interface supports:

- eDP 1.3 specification
- Spread-Spectrum Clocking
- eDP display authentication

Note

[1] *The conga-TCV2 supports either LVDS (default) or eDP (assembly option).*

[2] *The eDP interface does not support HDCP*

5.1.4 SATA

The conga-TCV2 offers two SATA ports. The first SATA port can be routed to SATA port 0 or SATA port 2 on the COM Express® connector. The second SATA port can be routed to SATA port 1 or SATA port 3 on the COM Express® connector. To set the active COM Express® SATA ports, use the BIOS setup menu.

The SATA interfaces support:

- data transfer rates up to 6.0 Gb/s
- AHCI mode Hot-plug detect

Note

The interfaces do not support legacy mode using I/O space.

5.1.5 USB

The conga-TCV2 offers eight USB ports (four USB 2.0 and four USB 3.1 Gen 2). The xHCI host controller supports:

- USB 3.1 specification
- SuperSpeedPlus, SuperSpeed, High-Speed, Full-Speed and Low-Speed USB signaling
- data transfers of up to 10 Gbps for USB 3.1 Gen 2 port
- data transfers of up to 5 Gbps for USB 3.1 Gen 1 port

Note

The USB ports are configured in the BIOS setup menu to operate by default in Gen 1 mode. Before you change the default setting to Gen 2, ensure the carrier board is designed for Gen 2 operation. For Gen 2 design considerations, contact congatec technical support center.

5.1.6 Gigabit Ethernet

The conga-TCV2 offers a 2.5 Gigabit Ethernet [1] interface via an onboard Intel® i225V controller. The interface supports:

- full-duplex operation at 10/100/1000/2500 Mbps [2, 3]
- half-duplex operation at 10/100 Mbps [2, 3]

Note

[1] *The MAC address of the Intel i225 Ethernet controller is preprogrammed by default. The MAC address cannot be reprogrammed. If you require custom MAC address, contact your local sales representative.*

[2] *The GBE0_LINK# output is not active during a 10 Mb connection. It is only active during a 100 Mb, 1 Gb or 2.5 Gb connection. This is a limitation of Ethernet controller since it only has 3 LED outputs—ACT#, LINK100# and LINK1000#.*

[3] *The GBE0_LINK# signal is a logic AND of the GBE0_LINK100# and GBE0_LINK1000# signals on the conga-TCV2 module. The LINK1000# output is active during 1 Gb and 2.5 Gb connection. The ACT# output is active during LINK#, LINK100# and LINK1000# (all speed). The LEDs blink when an activity is detected.*

5.1.7 High Definition Audio (HDA)

The conga-TCV2 provides an HD audio interface for up to three HDA codecs on the A–B connector.

5.1.8 LPC Bus

The conga-TCV2 offers the LPC (Low Pin Count) bus through the AMD Embedded Ryzen V2000 SoC. For information about the decoded LPC addresses, see section 9 "System Resources".

5.1.9 I²C Bus

The I²C bus is implemented through the congatec board controller and accessed through the congatec CGOS driver and API. The controller provides a fast-mode multi-master I²C bus that has the maximum I²C bandwidth.

5.1.10 SMBus

The SMBus is implemented through the congatec board controller and accessed through the congatec CGOS driver and API.

5.1.11 SPI

The SPI bus interface supports single and dual SPI interfaces with speeds up to 16 MHz. The conga-TCV2 discrete SPI TPM and the congatec BIOS flash are connected on the SPI interface.

Note

The SPI bus is for external BIOS flash only.

5.1.12 GPIO

The conga-TCV2 offers General Purpose Input/Output signals on the A–B connector. The GPIO signals are controlled by the congatec Board controller.

5.1.13 General Purpose Serial Interface

The conga-TCV2 offers two standard 16C550 UARTs on the A–B connector via the congatec Board Controller. The interfaces support up to 115200 baud rate.

Note

The UART interfaces do not support hardware handshake and flow control.

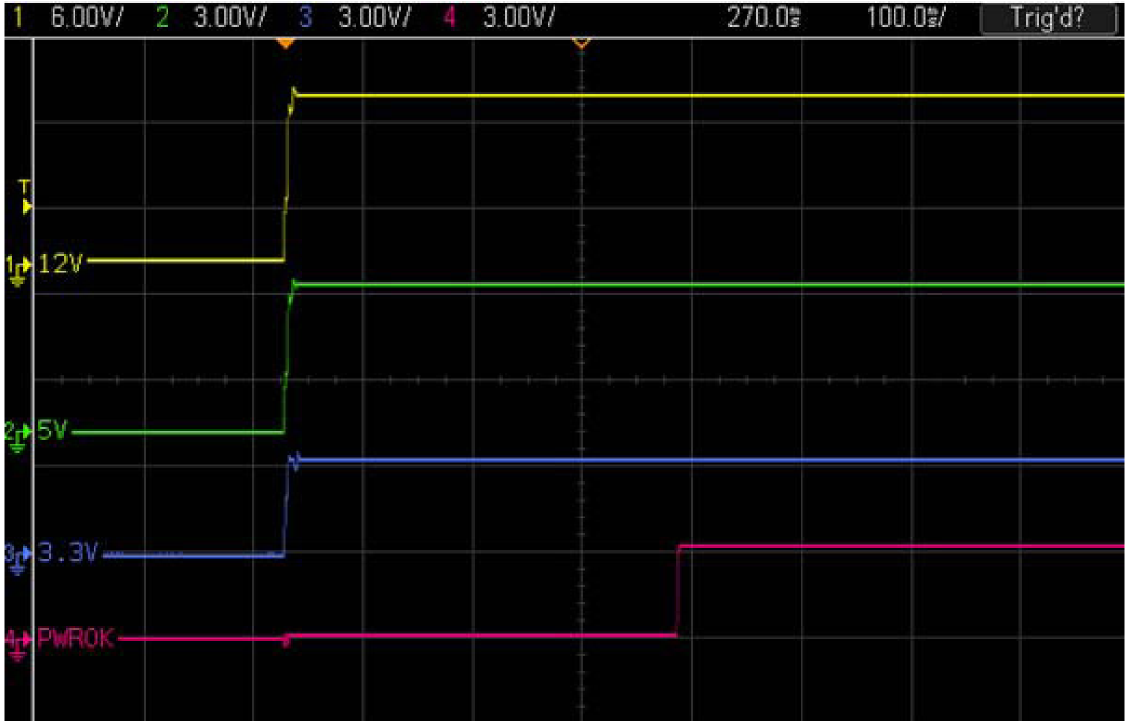
5.1.14 Power Control

PWR_OK

Power OK from main power supply or carrier board voltage regulator circuitry. A high value indicates that the power is good and the module can start its onboard power sequencing.

Carrier board hardware must drive this signal low until all power rails and clocks are stable. Releasing PWR_OK too early or not driving it low at all can cause numerous boot up problems. It is a good design practice to delay the PWR_OK signal a little (typically 100ms) after all carrier board power rails are up, to ensure a stable system.

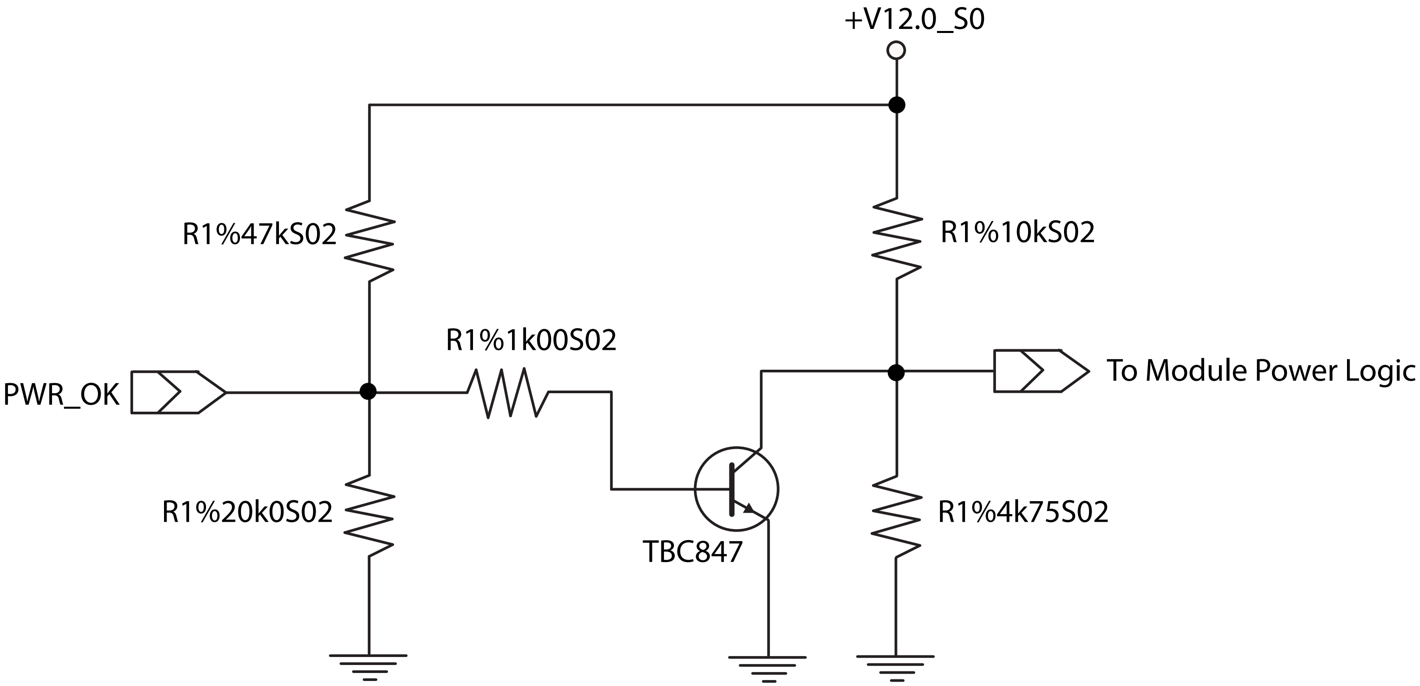
A sample screenshot is shown below:



Note

The module is kept in reset as long as the PWR_OK is driven by carrier board hardware.

The conga-TCV2 PWR_OK input circuitry is implemented as shown below:



The voltage divider ensures that the input complies with 3.3 V CMOS characteristic and also makes it possible to use the module on carrier board designs that do not drive the PWR_OK signal. Although the PWR_OK input is not mandatory for the onboard power-up sequencing, it is strongly recommended that the carrier board hardware drives the signal low until it is safe to let the module boot-up.

When considering the above shown voltage divider circuitry and the transistor stage, the voltage measured at the PWR_OK input pin may be only around 0.8 V when the 12 V is applied to the module. Actively driving PWR_OK high is compliant to the COM Express® specification but this can cause back driving. Therefore, congatec recommends driving the PWR_OK low to keep the module in reset and tri-state PWR_OK when the carrier board hardware is ready to boot.

The three typical usage scenarios for a carrier board design are:

- Connect PWR_OK to the "power good" signal of an ATX type power supply.
- Connect PWR_OK to the last voltage regulator in the chain on the carrier board.
- Simply pull PWR_OK with a 1k resistor to the carrier board 3.3 V power rail.

With this solution, you must ensure that by the time the 3.3 V is up, all carrier board hardware is fully powered and all clocks are stable.

The conga-TCV2 supports the controlling of ATX-style power supplies. If you do not use an ATX power supply, do not connect the conga-TCV2 pins SUS_S3/PS_ON, 5V_SB, and PWRBTN#.

SUS_S3#/PS_ON#

The SUS_S3#/PS_ON# (pin A15 on the A–B connector) signal is an active-low output that can be used to turn on the main outputs of an ATX-style power supply. To accomplish this the signal must be inverted with an inverter/transistor that is supplied by standby voltage and is located on the carrier board.

PWRBTN#

When using ATX-style power supplies, PWRBTN# (pin B12 on the A–B connector) is used to connect to a momentary-contact, active-low debounced push-button input while the other terminal on the push-button must be connected to ground. This signal is internally pulled up to 3V_SB using a 10 kΩ resistor. When PWRBTN# is asserted it indicates that an operator wants to turn the power on or off. The response to this signal from the system may vary as a result of modifications made in BIOS settings or by system software.

Power Supply Implementation Guidelines

The 12 V input power is the sole operational power source for the conga-TCV2. Other required voltages are generated internally on the module using onboard voltage regulators.

Note

When designing a power supply for a conga-TCV2 application, be aware that the system may malfunction when a 12 V power supply that produces non-monotonic voltage is used to power the system up. Though this problem is rare, it has been observed in some mobile power supply applications.

This problem occurs because some internal circuits on the module (e.g. clock-generator chips) generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused, thereby resulting in a malfunction.

To ensure this problem does not occur, observe the power supply rise waveform through an oscilloscope during the power supply qualification phase. This will help to determine if the rise is indeed monotonic and does not have any dips. For more information, see the "Power Supply Design Guide for Desktop Platform Form Factors" document at www.intel.com.

5.1.15 Power Management

ACPI

The conga-TCV2 supports Advanced Configuration and Power Interface (ACPI) specification, revision 5.0. It also supports Suspend to RAM (S3). For more information, see section 7.3 "ACPI Suspend Modes and Resume Events".

S5e Power State

The conga-TCV2 features a congatec proprietary Enhanced Soft-Off power state. See section 6.2.5 "Enhanced Soft-Off State" for more information.

6 Additional Features

The following features are available on the conga-TCV2.

6.1 TPM

The conga-TCV2 offers a discrete SPI TPM 2.0 (Infineon SLB9670VQ2.0) by default.

6.2 congatec Board Controller (cBC)

The conga-TCV2 is equipped with Microchip microcontroller. This onboard microcontroller plays an important role for most of the congatec embedded/industrial PC features. It fully isolates some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, which results in higher embedded feature performance and more reliability, even when the x86 processor is in a low power mode. It also ensures that the congatec embedded feature set is fully compatible amongst all congatec modules.

The board controller supports the following features:

- Board information
- Watchdog
- Power loss control
- General Purpose Input/Output (see section 5.1.12 "GPIO")
- I²C bus (see section 5.1.9 "I²C Bus"
- SMBus (see section 5.1.10 "SMBus")
- UART (see section 5.1.13 "General Purpose Serial Interface")
- Fan control
- Enhanced soft-off state (S5e)

6.2.1 Board Information

The cBC provides a rich data-set of manufacturing and board information such as serial number, EAN number, hardware and firmware revisions, and so on. It also keeps track of dynamically changing data like runtime meter and boot counter.

6.2.2 Watchdog

The conga-TCV2 is equipped with a multi stage watchdog solution that is triggered by software. For more information about the Watchdog feature, see the application note AN3_Watchdog.pdf on the congatec GmbH website at www.congatec.com.

Note

The conga-TCV2 module does not support the watchdog NMI mode.

6.2.3 Power Loss Control

The cBC provides the power loss control feature. The power loss control feature determines the behaviour of the system after an AC power loss occurs. This feature applies to systems with ATX-style power supplies which support standby power rail.

The term "power loss" implies that all power sources, including the standby power are lost (G3 state). Once power loss (transition to G3) or shutdown (transition to S5) occurs, the board controller continuously monitors the standby power rail. If the standby voltage remains stable for 30 seconds, the cBC assumes the system was switched off properly. If the standby voltage is no longer detected within 30 seconds, the module considers this an AC power loss condition.

The power loss control feature has three different modes that define how the system responds when standby power is restored after a power loss occurs. The modes are:

- Turn On: The system is turned on after a power loss condition
- Remain Off: The system is kept off after a power loss condition
- Last State: The board controller restores the last state of the system before the power loss condition

Note

1. *If a power loss condition occurs within 30 seconds after a regular shutdown, the cBC may incorrectly set the last state to "ON".*

2. *The settings for power loss control have no effect on systems with AT-style power supplies which do not support standby power rail.*

3. *The 30 seconds monitoring cycle applies only to the "Last State" power loss control mode.*

6.2.4 Fan Control

The conga-TCV2 has additional signals and functions to further improve system management. One of these signals is FAN_PWMOUT, an output signal that allows system fan control using a PWM (Pulse Width Modulation) output. Additionally, there is an input signal called FAN_TACHOIN that provides the ability to monitor the system's fan RPMs (revolutions per minute). This signal must receive two pulses per revolution in order to produce an accurate reading. For this reason, a two pulse per revolution fan or similar hardware solution is recommended.

Note

1. *A four wire fan must be used to generate the correct speed readout.*
2. *For the correct fan control (FAN_PWMOUT, FAN_TACHIN) implementation, see the COM Express® Design Guide.*

6.2.5 Enhanced Soft-Off State

The conga-TCV2 supports an enhanced Soft-Off state (S5e)—a congatec proprietary low-power Soft-Off state. In this state, the CPU module switches off almost all the onboard logic in order to reduce the power consumption to absolute minimum (between 0.05 mA and 0.125 mA).

Refer to congatec application note AN36_S5e_Implementation.pdf for detailed description of the S5e state.

6.3 OEM BIOS Customization

The conga-TCV2 is equipped with congatec Embedded BIOS, which is based on American Megatrends Inc. Aptio UEFI firmware. The congatec Embedded BIOS allows system designers to modify the BIOS. For more information about customizing the congatec Embedded BIOS, refer to the congatec System Utility user's guide CGUTLm1x.pdf on the congatec website at www.congatec.com or contact technical support.

The customization features supported are described below:

6.3.1 OEM Default Settings

This feature allows system designers to create and store their own BIOS default configuration. Customized BIOS development by congatec for OEM default settings is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_OEM_Default_Map.pdf on the congatec website for details on how to add OEM default settings to the congatec Embedded BIOS.

6.3.2 OEM Boot Logo

This feature allows system designers to replace the standard text output displayed during POST with their own BIOS boot logo. Customized BIOS development by congatec for OEM Boot Logo is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_And_Add_Bootlogo.pdf on the congatec website for details on how to add OEM boot logo to the congatec Embedded BIOS.

6.3.3 OEM POST Logo

This feature allows system designers to replace the congatec POST logo displayed in the upper left corner of the screen during BIOS POST with their own BIOS POST logo. Use the congatec system utility CGUTIL 1.5.4 or later to replace/add the OEM POST logo.

6.3.4 OEM DXE Driver

This feature allows designers to add their own UEFI DXE driver to the congatec embedded BIOS. Contact congatec technical support for more information on how to add an OEM DXE driver.

6.4 congatec Battery Management Interface

To facilitate the development of battery powered mobile systems based on embedded modules, congatec GmbH defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (for example, charge state of the battery, information about the battery, alarms/events for certain battery states and so on) without the need for additional modifications to the system BIOS.

In addtion to the ACPI-Compliant Control Method Battery mentioned above, the latest versions of the conga-TCV2 BIOS and board controller firmware also support LTC1760 battery manager from Linear Technology and a battery only solution (no smart battery system manager). All three battery solutions are supported on the I2C bus and the SMBus. This gives the system designer more flexibility when choosing the appropriate battery sub-system. For more information about the supported Battery Management Interface, contact your local sales representative.

6.5 API Support (CGOS)

In order to benefit from the above mentioned non-industry standard feature set, congatec provides an API that allows application software developers to easily integrate all these features into their code. The CGOS API (congatec Operating System Application Programming Interface) is the congatec proprietary API that is available for all commonly used Operating Systems such as Win32, Win64, Win CE, Linux.

The architecture of the CGOS API driver provides the ability to write application software that runs unmodified on all congatec CPU modules. All the hardware related code is contained within the congatec embedded BIOS on the module. See section 1.1 of the CGOS API software developers guide, available on the congatec website.

6.6 Suspend to Ram

The Suspend to RAM feature is available on the conga-TCV2.

7 conga Tech Notes

The conga-TCV2 has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features

7.1 AMD Processor Features

The Zen2 microarchitecture supports the following:

- 7 nm FinFET technology
- Up to eight cores/16 threads
- Configurable TDP options as low as 10 W
- New TAGE branch predictor
- Reoptimzed L1 cache
- 32K, 8-way L1 cache
- 512K, 8-way L2 cache
- 2x FP data path width
- User Mode Instruction Prevention (UMIP)
- APIC extension for high core count system support
- Cache-line Writeback (CLWB)
- Processor register read at a user level
- Quality of service monitoring
- Improved prefetch throttling

For more information about AMD Technology, visit http://www.amd.com.

7.2 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system's thermal management. This results in the operating system having the ability to take control of the operating environment by implementing cooling decisions according to the demands put on the CPU by the application.

The conga-TCV2 ACPI thermal solution offers three different cooling policies:

- **Passive Cooling**

When the temperature in the thermal zone must be reduced, the operating system can decrease the power consumption of the processor by throttling the processor clock. One of the advantages of this cooling policy is that passive cooling devices (in this case the processor) do not produce any noise. Use the "passive cooling trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start or stop the passive cooling procedure.

- **Active Cooling**

During this cooling policy the operating system is turning the fan on/off. Although active cooling devices consume power and produce noise, they also have the ability to cool the thermal zone without having to reduce the overall system performance. Use the "active cooling trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start the active cooling device. It is stopped again when the temperature goes below the threshold (5°C hysteresis).

- **Critical Trip Point**

If the temperature in the thermal zone reaches a critical point then the operating system will perform a system shut down in an orderly fashion in order to ensure that there is no damage done to the system as result of high temperatures. Use the "critical trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to shut down the system

Note

The end user must determine the cooling preferences for the system by using the setup nodes in the BIOS setup program to establish the appropriate trip points. If passive cooling is activated and the processor temperature is above the trip point the processor clock is throttled. See section 12 of the ACPI Specification 2.0 C for more information about passive cooling.

7.3 ACPI Suspend Modes and Resume Events

The conga-TCV2 BIOS supports S3 (Suspend to RAM), S4 (Suspend to Disk) and S5 (Soft-Off).

Table 11 Wake Events

The table below lists the events that wake the system from S3-S5.

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S3-S5 and S5e
Onboard LAN Event	Device driver must be configured for Wake On LAN support
SMBALERT#	Wakes unconditionally from S3-S5
PCI Express WAKE#	Wakes unconditionally from S3-S5
WAKE#	Wakes unconditionally from S3
PME#	Activate the wake up capabilities of a PCI device using Windows Device Manager configuration options for this device OR set Resume On PME# to Enabled in the Power setup menu
USB Mouse/Keyboard Event	When Standby mode is set to S3, USB hardware must be powered by standby power source. Set USB Device Wakeup from S3/S4 to ENABLED in the ACPI setup menu (if setup node is available in BIOS setup program). In Device Manager look for the keyboard/mouse devices. Go to the Power Management tab and check 'Allow this device to bring the computer out of standby'
RTC Alarm	Activate and configure Resume On RTC Alarm in the Power setup menu. Only available in S5
Watchdog Power Button Event	Wakes unconditionally from S3-S5

8 Signal Descriptions and Pinout Tables

The following section describes the signals found on COM Express® Type 6 connectors used for congatec GmbH modules. The pinout of the modules complies with COM Express® Type 6, rev. 3.0.

The table below describes the terminology used in this section. The PU/PD column indicates if a pull-up or pull-down resistor has been used. If the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented by congatec.

The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

Table 12 Signal Tables Terminology Descriptions

Term	Description
PU	Implemented pull-up resistor
PD	Implemented pull-down resistor
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
I/O 3.3VSB	Input or output 3.3V tolerant active in standby state
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
OD	Open drain output
P	Power Input/Output
DDC	Display Data Channel
PCIe	PCI Express compatible differential signal
DP	DisplayPort compatible differential signal
PEG	PCI Express Graphics
SATA	In compliance with Serial ATA specification Revision 2.6 and 3.0
LVDS	Low Voltage Differential Signal
PDS	Pull-down strap. A module output pin that is either tied to GND or is not connected. Used to signal module capabilities (pinout type) to the Carrier Board

8.1 A-B Connector Signal Descriptions

Table 13 Connector A–B Pinout

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A1	GND (FIXED)	B1	GND (FIXED)	A56	PCIE_TX4-	B56	PCIE_RX4-
A2	GBE0_MDI3-	B2	GBE0_ACT#	A57	GND	B57	GPO2
A3	GBE0_MDI3+	B3	LPC_FRAME#	A58	PCIE_TX3+	B58	PCIE_RX3+
A4	GBE0_LINK100#	B4	LPC_AD0	A59	PCIE_TX3-	B59	PCIE_RX3-
A5	GBE0_LINK1000#	B5	LPC_AD1	A60	GND (FIXED)	B60	GND (FIXED)
A6	GBE0_MDI2-	B6	LPC_AD2	A61	PCIE_TX2+	B61	PCIE_RX2+
A7	GBE0_MDI2+	B7	LPC_AD3	A62	PCIE_TX2-	B62	PCIE_RX2-
A8	GBE0_LINK#	B8	LPC_DRQ0#	A63	GPI1	B63	GPO3
A9	GBE0_MDI1-	B9	LPC_DRQ1#[1]	A64	PCIE_TX1+	B64	PCIE_RX1+
A10	GBE0_MDI1+	B10	LPC_CLK	A65	PCIE_TX1-	B65	PCIE_RX1-
A11	GND (FIXED)	B11	GND (FIXED)	A66	GND	B66	WAKE0#
A12	GBE0_MDI0-	B12	PWRBTN#	A67	GPI2	B67	WAKE1#
A13	GBE0_MDI0+	B13	SMB_CK	A68	PCIE_TX0+	B68	PCIE_RX0+
A14	GBE0_CTREF [1]	B14	SMB_DAT	A69	PCIE_TX0-	B69	PCIE_RX0-
A15	SUS_S3#	B15	SMB_ALERT#	A70	GND (FIXED)	B70	GND (FIXED)
A16	SATA0_TX+	B16	SATA1_TX+	A71	eDP_TX2+ / LVDS_A0+	B71	LVDS_B0+
A17	SATA0_TX-	B17	SATA1_TX-	A72	eDP_TX2- / LVDS_A0-	B72	LVDS_B0-
A18	SUS_S4#	B18	SUS_STAT#	A73	eDP_TX1+ / LVDS_A1+	B73	LVDS_B1+
A19	SATA0_RX+	B19	SATA1_RX+	A74	eDP_TX1- / LVDS_A1-	B74	LVDS_B1-
A20	SATA0_RX-	B20	SATA1_RX-	A75	eDP_TX0+ / LVDS_A2+	B75	LVDS_B2+
A21	GND (FIXED)	B21	GND (FIXED)	A76	eDP_TX0- / LVDS_A2-	B76	LVDS_B2-
A22	SATA2_TX+	B22	SATA3_TX+	A77	eDP_VDD_EN/LVDS_VDD_EN	B77	LVDS_B3+
A23	SATA2_TX-	B23	SATA3_TX-	A78	LVDS_A3+	B78	LVDS_B3-
A24	SUS_S5#	B24	PWR_OK	A79	LVDS_A3-	B79	eDP_BKLT_EN/LVDS_BKLT_EN
A25	SATA2_RX+	B25	SATA3_RX+	A80	GND (FIXED)	B80	GND (FIXED)
A26	SATA2_RX-	B26	SATA3_RX-	A81	eDP_TX3+ / LVDS_A_CK+	B81	LVDS_B_CK+
A27	BATLOW#	B27	WDT	A82	eDP_TX3- / LVDS_A_CK-	B82	LVDS_B_CK-
A28	(S)ATA_ACT#	B28	HDA_SDIN2	A83	eDP_ AUX+ / LVDS_I2C_CK	B83	eDP/LVDS_BKLT_CTRL
A29	HDA_SYNC	B29	HDA_SDIN1	A84	eDP_AUX- / LVDS_I2C_DAT	B84	VCC_5V_SBY
A30	HDA_RST#	B30	HDA_SDIN0	A85	GPI3	B85	VCC_5V_SBY

Pin	Row A	Pin	Row B	Pin	Row A	Pin	Row B
A31	GND (FIXED)	B31	GND (FIXED)	A86	RSVD [1]	B86	VCC_5V_SBY
A32	HDA_BITCLK	B32	SPKR	A87	eDP_HPD	B87	VCC_5V_SBY
A33	HDA_SDOUT	B33	I2C_CK	A88	PCIE_CLK_REF+	B88	BIOS_DIS1#
A34	BIOS_DIS0#	B34	I2C_DAT	A89	PCIE_CLK_REF-	B89	VGA_RED [2]
A35	THRMTRIP#	B35	THRM#	A90	GND (FIXED)	B90	GND (FIXED)
A36	USB6-	B36	USB7-	A91	SPI_POWER	B91	VGA_GRN [2]
A37	USB6+	B37	USB7+	A92	SPI_MISO	B92	VGA_BLU [2]
A38	USB_6_7_OC#	B38	USB_4_5_OC#	A93	GPO0	B93	VGA_HSYNC [2]
A39	USB4-	B39	USB5-	A94	SPI_CLK	B94	VGA_VSYNC [2]
A40	USB4+	B40	USB5+	A95	SPI_MOSI	B95	VGA_I2C_CK [1]
A41	GND (FIXED)	B41	GND (FIXED)	A96	TPM_PP	B96	VGA_I2C_DAT [1]
A42	USB2-	B42	USB3-	A97	TYPE10# [1]	B97	SPI_CS#
A43	USB2+	B43	USB3+	A98	SER0_TX	B98	RSVD [1]
A44	USB_2_3_OC#	B44	USB_0_1_OC#	A99	SER0_RX	B99	RSVD [1]
A45	USB0-	B45	USB1-	A100	GND (FIXED)	B100	GND (FIXED)
A46	USB0+	B46	USB1+	A101	SER1_TX	B101	FAN_PWMOUT
A47	VCC_RTC	B47	ESPI_EN# [1]	A102	SER1_RX	B102	FAN_TACHIN
A48	RSVD [1]	B48	USB0_HOST_PRSNT [1]	A103	LID#	B103	SLEEP#
A49	GBE0_SDP	B49	SYS_RESET#	A104	VCC_12V	B104	VCC_12V
A50	LPC_SERIRQ	B50	CB_RESET#	A105	VCC_12V	B105	VCC_12V
A51	GND (FIXED)	B51	GND (FIXED)	A106	VCC_12V	B106	VCC_12V
A52	PCIE_TX5+	B52	PCIE_RX5+	A107	VCC_12V	B107	VCC_12V
A53	PCIE_TX5-	B53	PCIE_RX5-	A108	VCC_12V	B108	VCC_12V
A54	GPI0	B54	GPO1	A109	VCC_12V	B109	VCC_12V
A55	PCIE_TX4+	B55	PCIE_RX4+	A110	GND (FIXED)	B110	GND (FIXED)

Note

1. *Not connected*
2. *Not supported*

Table 14 Connector C–D Pinout

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C1	GND (FIXED)	D1	GND (FIXED)	C56	PEG_RX1-	D56	PEG_TX1-
C2	GND	D2	GND	C57	TYPE1# [1]	D57	TYPE2#
C3	USB_SSRX0-	D3	USB_SSTX0-	C58	PEG_RX2+	D58	PEG_TX2+
C4	USB_SSRX0+	D4	USB_SSTX0+	C59	PEG_RX2-	D59	PEG_TX2-
C5	GND	D5	GND	C60	GND (FIXED)	D60	GND (FIXED)
C6	USB_SSRX1-	D6	USB_SSTX1-	C61	PEG_RX3+	D61	PEG_TX3+
C7	USB_SSRX1+	D7	USB_SSTX1+	C62	PEG_RX3-	D62	PEG_TX3-
C8	GND	D8	GND	C63	RSVD [3]	D63	RSVD [1]
C9	USB_SSRX2-	D9	USB_SSTX2-	C64	RSVD [3] (see caution below)	D64	RSVD [1]
C10	USB_SSRX2+	D10	USB_SSTX2+	C65	PEG_RX4+	D65	PEG_TX4+
C11	GND (FIXED)	D11	GND (FIXED)	C66	PEG_RX4-	D66	PEG_TX4-
C12	USB_SSRX3-	D12	USB_SSTX3-	C67	RAPID_SHUTDOWN [1,2]	D67	GND
C13	USB_SSRX3+	D13	USB_SSTX3+	C68	PEG_RX5+	D68	PEG_TX5+
C14	GND	D14	GND	C69	PEG_RX5-	D69	PEG_TX5-
C15	DDI1_PAIR6+ [1]	D15	DDI1_CTRLCLK_AUX+	C70	GND (FIXED)	D70	GND (FIXED)
C16	DDI1_PAIR6- [1]	D16	DDI1_CTRLDATA_AUX-	C71	PEG_RX6+	D71	PEG_TX6+
C17	RSVD [1]	D17	RSVD [1]	C72	PEG_RX6-	D72	PEG_TX6-
C18	RSVD [1]	D18	RSVD [1]	C73	GND	D73	GND
C19	PCIE_RX6+	D19	PCIE_TX6+	C74	PEG_RX7+	D74	PEG_TX7+
C20	PCIE_RX6-	D20	PCIE_TX6-	C75	PEG_RX7-	D75	PEG_TX7-
C21	GND (FIXED)	D21	GND (FIXED)	C76	GND	D76	GND
C22	PCIE_RX7+	D22	PCIE_TX7+	C77	RSVD [1]	D77	RSVD [1]
C23	PCIE_RX7-	D23	PCIE_TX7-	C78	PEG_RX8+ [1]	D78	PEG_TX8+ [1]
C24	DDI1_HPD	D24	RSVD [1]	C79	PEG_RX8- [1]	D79	PEG_TX8- [1]
C25	DDI1_PAIR4+ [1]	D25	RSVD [1]	C80	GND (FIXED)	D80	GND (FIXED)
C26	DDI1_PAIR4- [1]	D26	DDI1_PAIR0+	C81	PEG_RX9+ [1]	D81	PEG_TX9+ [1]
C27	RSVD [1]	D27	DDI1_PAIR0-	C82	PEG_RX9- [1]	D82	PEG_TX9- [1]
C28	RSVD [1]	D28	RSVD [1]	C83	RSVD [1]	D83	RSVD [1]
C29	DDI1_PAIR5+ [1]	D29	DDI1_PAIR1+	C84	GND	D84	GND
C30	DDI1_PAIR5- [1]	D30	DDI1_PAIR1-	C85	PEG_RX10+ [1]	D85	PEG_TX10+ [1]
C31	GND (FIXED)	D31	GND (FIXED)	C86	PEG_RX10- [1]	D86	PEG_TX10- [1]
C32	DDI2_CTRLCLK_AUX+	D32	DDI1_PAIR2+	C87	GND	D87	GND

Pin	Row C	Pin	Row D	Pin	Row C	Pin	Row D
C33	DDI2_CTRLDATA_AUX-	D33	DDI1_PAIR2-	C88	PEG_RX11+[1]	D88	PEG_TX11+[1]
C34	DDI2_DDC_AUX_SEL	D34	DDI1_DDC_AUX_SEL	C89	PEG_RX11-[1]	D89	PEG_TX11-[1]
C35	RSVD[1]	D35	RSVD[1]	C90	GND (FIXED)	D90	GND (FIXED)
C36	DDI3_CTRLCLK_AUX+	D36	DDI1_PAIR3+	C91	PEG_RX12+[1]	D91	PEG_TX12+[1]
C37	DDI3_CTRLDATA_AUX-	D37	DDI1_PAIR3-	C92	PEG_RX12-[1]	D92	PEG_TX12-[1]
C38	DDI3_DDC_AUX_SEL	D38	RSVD[1]	C93	GND	D93	GND
C39	DDI3_PAIR0+	D39	DDI2_PAIR0+	C94	PEG_RX13+[1]	D94	PEG_TX13+[1]
C40	DDI3_PAIR0-	D40	DDI2_PAIR0-	C95	PEG_RX13-[1]	D95	PEG_TX13-[1]
C41	GND (FIXED)	D41	GND (FIXED)	C96	GND	D96	GND
C42	DDI3_PAIR1+	D42	DDI2_PAIR1+	C97	RVSD[1]	D97	RSVD[1]
C43	DDI3_PAIR1-	D43	DDI2_PAIR1-	C98	PEG_RX14+[1]	D98	PEG_TX14+[1]
C44	DDI3_HPD	D44	DDI2_HPD	C99	PEG_RX14-[1]	D99	PEG_TX14-[1]
C45	RSVD[1]	D45	RSVD[1]	C100	GND (FIXED)	D100	GND (FIXED)
C46	DDI3_PAIR2+	D46	DDI2_PAIR2+	C101	PEG_RX15+[1]	D101	PEG_TX15+[1]
C47	DDI3_PAIR2-	D47	DDI2_PAIR2-	C102	PEG_RX15-[1]	D102	PEG_TX15-[1]
C48	RSVD	D48	RSVD[1]	C103	GND	D103	GND
C49	DDI3_PAIR3+	D49	DDI2_PAIR3+	C104	VCC_12V	D104	VCC_12V
C50	DDI3_PAIR3-	D50	DDI2_PAIR3-	C105	VCC_12V	D105	VCC_12V
C51	GND (FIXED)	D51	GND (FIXED)	C106	VCC_12V	D106	VCC_12V
C52	PEG_RX0+	D52	PEG_TX0+	C107	VCC_12V	D107	VCC_12V
C53	PEG_RX0-	D53	PEG_TX0-	C108	VCC_12V	D108	VCC_12V
C54	TYPE0#[1]	D54	PEG_LANE_RV#[1]	C109	VCC_12V	D109	VCC_12V
C55	PEG_RX1+	D55	PEG_TX1+	C110	GND (FIXED)	D110	GND (FIXED)

Note

[1] *Not connected*

[2] *Not supported*

[3] *congatec internal use only*

Caution

Using the conga-TCV2 on a COM Express 3.1 carrier board may cause functionality issues. Pin C64 (defined as RSVD in COM Express 3.0) is used for cBC diagnostic output. This pin is defined as GND in COM Express 3.1 specification.

Table 15 PCI Express Signal Descriptions (general purpose)

Signal	Pin #	Description	I/O	PU/PD	Comment
PCIE_RX0+ PCIE_RX0-	B68 B69	PCI Express channel 0, Receive Input differential pair	I PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_TX0+ PCIE_TX0-	A68 A69	PCI Express channel 0, Transmit Output differential pair	O PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_RX1+ PCIE_RX1-	B64 B65	PCI Express channel 1, Receive Input differential pair	I PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_TX1+ PCIE_TX1-	A64 A65	PCI Express channel 1, Transmit Output differential pair	O PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_RX2+ PCIE_RX2-	B61 B62	PCI Express channel 2, Receive Input differential pair	I PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_TX2+ PCIE_TX2-	A61 A62	PCI Express channel 2, Transmit Output differential pair	O PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_RX3+ PCIE_RX3-	B58 B59	PCI Express channel 3, Receive Input differential pair	I PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_TX3+ PCIE_TX3-	A58 A59	PCI Express channel 3, Transmit Output differential pair	O PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_RX4+ PCIE_RX4-	B55 B56	PCI Express channel 4, Receive Input differential pair	I PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_TX4+ PCIE_TX4-	A55 A56	PCI Express channel 4, Transmit Output differential pair	O PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_RX5+ PCIE_RX5-	B52 B53	PCI Express channel 5, Receive Input differential pair	I PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_TX5+ PCIE_TX5-	A52 A53	PCI Express channel 5, Transmit Output differential pair	O PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_RX6+ PCIE_RX6-	C19 C20	PCI Express channel 6, Receive Input differential pair	I PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_TX6+ PCIE_TX6-	D19 D20	PCI Express channel 6, Transmit Output differential pair	O PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_RX7+ PCIE_RX7-	C22 C23	PCI Express channel 7, Receive Input differential pair	I PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_TX7+ PCIE_TX7-	D22 D23	PCI Express channel 7, Transmit Output differential pair	O PCIE		Supports PCI Express Base Specification, Revision 3.0
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCI Express Reference Clock output for all PCI Express and PCI Express Graphics Lanes	O PCIE		A PCI Express Gen3 compliant clock buffer chip must be used on the carrier board if the design involves more than one PCI Express device

Table 16 PCI Express Signal Descriptions (x16 Graphics)

Signal	Pin #	Description	I/O	PU/PD	Comment
PEG_RX0+ PEG_RX0-	C52 C53	PCI Express Graphics differential pairs 0 *Note: Can also be used as PCI Express differential pairs 16*	I PCIE		PCI Express Gen 3
PEG_TX0+ PEG_TX0-	D52 D53		O PCIE		
PEG_RX1+ PEG_RX1-	C55 C56	PCI Express Graphics differential pairs 1 *Note: Can also be used as PCI Express differential pairs 17*	I PCIE		
PEG_TX1+ PEG_TX1-	D55 D56		O PCIE		
PEG_RX2+ PEG_RX2-	C58 C59	PCI Express Graphics differential pairs 2 *Note: Can also be used as PCI Express differential pairs 18*	I PCIE		
PEG_TX2+ PEG_TX2-	D58 D59		O PCIE		
PEG_RX3+ PEG_RX3-	C61 C62	PCI Express Graphics differential pairs 3 *Note: Can also be used as PCI Express differential pairs 19*	I PCIE		
PEG_TX3+ PEG_TX3-	D61 D62		O PCIE		
PEG_RX4+ PEG_RX4-	C65 C66	PCI Express Graphics differential pairs 4 *Note: Can also be used as PCI Express differential pairs 20*	I PCIE		
PEG_TX4+ PEG_TX4-	D65 D66		O PCIE		
PEG_RX5+ PEG_RX5-	C68 C69	PCI Express Graphics differential pairs 5 *Note: Can also be used as PCI Express differential pairs 21*	I PCIE		
PEG_TX5+ PEG_TX5-	D68 D69		O PCIE		
PEG_RX6+ PEG_RX6-	C71 C72	PCI Express Graphics differential pairs 6 *Note: Can also be used as PCI Express differential pairs 22*	I PCIE		
PEG_TX6+ PEG_TX6-	D71 D72		O PCIE		
PEG_RX7+ PEG_RX7-	C74 C75	PCI Express Graphics differential pairs 7 *Note: Can also be used as PCI Express differential pairs 23*	I PCIE		
PEG_TX7+ PEG_TX7-	D74 D75		O PCIE		
PEG_RX8+ PEG_RX8-	C78 C79	PCI Express Graphics differential pairs 8 *Note: Can also be used as PCI Express differential pairs 24*	I PCIE		Not connected
PEG_TX8+ PEG_TX8-	D78 D79		O PCIE		
PEG_RX9+ PEG_RX9-	C81 C82	PCI Express Graphics differential pairs 9 *Note: Can also be used as PCI Express differential pairs 25*	I PCIE		
PEG_TX9+ PEG_TX9-	D81 D82		O PCIE		

Signal	Pin #	Description	I/O	PU/PD	Comment
PEG_RX10+ PEG_RX10-	C85 C86	PCI Express Graphics differential pairs 10 *Note: Can also be used as PCI Express differential pairs 26*		I PCIE	Not connected
PEG_TX10+ PEG_TX10-	D85 D86			O PCIE	
PEG_RX11+ PEG_RX11-	C88 C89	PCI Express Graphics differential pairs 11 *Note: Can also be used as PCI Express differential pairs 27*		I PCIE	
PEG_TX11+ PEG_TX11-	D88 D89			O PCIE	
PEG_RX12+ PEG_RX12-	C91 C92	PCI Express Graphics differential pairs 12 *Note: Can also be used as PCI Express differential pairs 28*		I PCIE	
PEG_TX12+ PEG_TX12-	D91 D92			O PCIE	
PEG_RX13+ PEG_RX13-	C94 C95	PCI Express Graphics differential pairs 13 *Note: Can also be used as PCI Express differential pairs 29*		I PCIE	
PEG_TX13+ PEG_TX13-	D94 D95			O PCIE	
PEG_RX14+ PEG_RX14-	C98 C99	PCI Express Graphics differential pairs 14 *Note: Can also be used as PCI Express differential pairs 30*		I PCIE	
PEG_TX14+ PEG_TX14-	D98 D99			O PCIE	
PEG_RX15+ PEG_RX15-	C101 C102	PCI Express Graphics differential pairs 15 *Note: Can also be used as PCI Express differential pairs 31*		I PCIE	
PEG_TX15+ PEG_TX15-	D101 D102			O PCIE	
PEG_LANE_RV#	D54	PCI Express Graphics lane reversal input strap. Pull low on the carrier board to reverse lane order.	I		Not supported

Note

The conga-TCV2 supports only PEG ports 0-7.

Table 17 DDI Signal Description

Signal	Pin #	Description	I/O	PU/PD	Comment
DDI1_PAIR0+ DDI1_PAIR0-	D26 D27	Multiplexed with DP1_LANE0+ and TMDS1_DATA2+ Multiplexed with DP1_LANE0- and TMDS1_DATA2-	O DP		Should be AC-coupled on the carrier board.
DDI1_PAIR1+ DDI1_PAIR1-	D29 D30	Multiplexed with DP1_LANE1+ and TMDS1_DATA1+ Multiplexed with DP1_LANE1- and TMDS1_DATA1-	O DP		
DDI1_PAIR2+ DDI1_PAIR2-	D32 D33	Multiplexed with DP1_LANE2+ and TMDS1_DATA0+ Multiplexed with DP1_LANE2- and TMDS1_DATA0-	O DP		
DDI1_PAIR3+ DDI1_PAIR3-	D36 D37	Multiplexed with DP1_LANE3+ and TMDS1_CLK+ Multiplexed with DP1_LANE3- and TMDS1_CLK-	O DP		
DDI1_HPD	C24	Multiplexed with DP1_HPD and HDMI1_HPD	I 3.3 V	PD 100 kΩ	
DDI1_CTRLCLK_AUX+	D15	Multiplexed with DP1_AUX+ and HMDI1_CTRLCLK DP AUX+ function if DDI1_DDC_AUX_SEL is no connect HDMI/DVI I2C CTRLCLK if DDI1_DDC_AUX_SEL is pulled high	I/O DP OD 3.3 V	PD 100 kΩ	For TMDS mode, 2.2K to 3.3V pull-up resistor should be implemented on the carrier board.
DDI1_CTRLDATA_AUX-	D16	Multiplexed with DP1_AUX- and HMDI1_CTRLDATA DP AUX- function if DDI1_DDC_AUX_SEL is no connect HDMI/DVI I2C CTRLDATA if DDI1_DDC_AUX_SEL is pulled high	I/O DP I/OD 3.3 V	PU 100 kΩ 3.3V	For TMDS mode, 2.2K to 3.3V pull-up resistor should be implemented on the carrier board.
DDI1_DDC_AUX_SEL	D34	Selects the function of DDI1_CTRLCLK_AUX+ and DDI1_CTRLDATA_AUX- This pin shall have a IM pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals.	I 3.3 V	PD 1 MΩ	
DDI2_PAIR0+ DDI2_PAIR0-	D39 D40	Multiplexed with DP2_LANE0+ and TMDS2_DATA2+ Multiplexed with DP2_LANE0- and TMDS2_DATA2-	O DP		Should be AC-coupled on the carrier board.
DDI2_PAIR1+ DDI2_PAIR1-	D42 D43	Multiplexed with DP2_LANE1+ and TMDS2_DATA1+ Multiplexed with DP2_LANE1- and TMDS2_DATA1-	O DP		
DDI2_PAIR2+ DDI2_PAIR2-	D46 D47	Multiplexed with DP2_LANE2+ and TMDS2_DATA0+ Multiplexed with DP2_LANE2- and TMDS2_DATA0-	O DP		
DDI2_PAIR3+ DDI2_PAIR3-	D49 D50	Multiplexed with DP2_LANE3+ and TMDS2_CLK+ Multiplexed with DP2_LANE3- and TMDS2_CLK-	O DP		
DDI2_HPD	D44	Multiplexed with DP2_HPD and HDMI2_HPD	I 3.3 V	PD 100 kΩ	
DDI2_CTRLCLK_AUX+	C32	Multiplexed with DP2_AUX+ and HDMI2_CTRLCLK DP AUX+ function if DDI2_DDC_AUX_SEL is no connect HDMI/DVI I2C CTRLCLK if DDI2_DDC_AUX_SEL is pulled high	I/O DP OD 3.3 V	PD 100 kΩ	For TMDS mode, 2.2K to 3.3V pull-up resistor should be implemented on the carrier board.
DDI2_CTRLDATA_AUX-	C33	Multiplexed with DP2_AUX- and HDMI2_CTRLDATA DP AUX- function if DDI2_DDC_AUX_SEL is no connect HDMI/DVI I2C CTRLDATA if DDI2_DDC_AUX_SEL is pulled high	I/O DP I/OD 3.3 V	PU 100 kΩ 3.3V	For TMDS mode, 2.2K to 3.3V pull-up resistor should be implemented on the carrier board.
DDI2_DDC_AUX_SEL	C34	Selects the function of DDI2_CTRLCLK_AUX+ and DDI2_CTRLDATA_AUX- This pin shall have a IM pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals.	I 3.3 V	PD 1 MΩ	
DDI3_PAIR0+ DDI3_PAIR0-	C39 C40	Multiplexed with DP3_LANE0+ and TMDS3_DATA2+ Multiplexed with DP3_LANE0- and TMDS3_DATA2-	O DP		Should be AC-coupled on the carrier board.

O DP

Signal	Pin #	Description	I/O	PU/PD	Comment
DDI3_PAIR1+ DDI3_PAIR1-	C42 C43	Multiplexed with DP3_LANE1+ and TMDS3_DATA1+ Multiplexed with DP3_LANE1- and TMDS3_DATA1-	O DP		Should be AC-coupled on the carrier board.
DDI3_PAIR2+ DDI3_PAIR2-	C46 C47	Multiplexed with DP3_LANE2+ and TMDS3_DATA0+ Multiplexed with DP3_LANE2- and TMDS3_DATA0-	O DP		
DDI3_PAIR3+ DDI3_PAIR3-	C49 C50	Multiplexed with DP3_LANE3+ and TMDS3_CLK+ Multiplexed with DP3_LANE3- and TMDS3_CLK-	O DP		
DDI3_HPD	C44	Multiplexed with DP3_HPD and HDMI3_HPD	I 3.3 V	PD 100 kΩ	
DDI3_CTRLCLK_AUX+	C36	Multiplexed with DP3_AUX+ and HDMI3_CTRLCLK DP AUX+ function if DDI3_DDC_AUX_SEL is no connect HDMI/DVI I2C CTRLCLK if DDI3_DDC_AUX_SEL is pulled high	I/O DP OD 3.3 V	PD 100 kΩ	For TMDS mode, 2.2K to 3.3V pull-up resistor should be implemented on the carrier board.
DDI3_CTRLDATA_AUX-	C37	Multiplexed with DP3_AUX- and HDMI3_CTRLDATA DP AUX- function if DDI3_DDC_AUX_SEL is no connect HDMI/DVI I2C CTRLDATA if DDI3_DDC_AUX_SEL is pulled high	I/O DP I/OD 3.3 V	PU 100 kΩ	For TMDS mode, 2.2K to 3.3V pull-up resistor should be implemented on the carrier board.
DDI3_DDC_AUX_SEL	C38	Selects the function of DDI3_CTRLCLK_AUX+ and DDI3_CTRLDATA_AUX- This pin shall have a 1 M pull-down to logic ground on the module. If this input is floating, the AUX pair is used for the DP AUX+/- signals. If pulled-high, the AUX pair contains the CTRLCLK and CTRLDATA signals.	I 3.3 V	PD 1 MΩ	

Note

The DDI interfaces support dual-mode DisplayPort. To support TMDS, an external level shifter (PTN3360D) should be implemented on the user's carrier board.

Table 18 TMDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
TMDS1_CLK + TMDS1_CLK -	D36 D37	TMDS Clock output differential pair. Multiplexed with DDI1_PAIR3+ and DDI1_PAIR3-	O DP		Should be AC-coupled on the carrier board.
TMDS1_DATA0+ TMDS1_DATA0-	D32 D33	TMDS differential pair. Multiplexed with DDI1_PAIR2+ and DDI1_PAIR2-	O DP		
TMDS1_DATA1+ TMDS1_DATA1-	D29 D30	TMDS differential pair. Multiplexed with DDI1_PAIR1+ and DDI1_PAIR1-	O DP		
TMDS1_DATA2+ TMDS1_DATA2-	D26 D27	TMDS differential pair. Multiplexed with DDI1_PAIR0+ and DDI1_PAIR0-	O DP		
HDMI1_HPD	C24	TMDS Hot-plug detect. Multiplexed with DDI1_HPD	I DP	PD 100 kΩ	
HDMI1_CTRLCLK	D15	TMDS I^{2}C Control Clock. Multiplexed with DDI1_CTRLCLK_AUX+	OD 3.3 V	PD 100 kΩ	2.2 kΩ to 3.3V pull-up should be implemented on the carrier board.
HDMI1_CTRLDATA	D16	TMDS I^{2}C Control Data Multiplexed with DDI1_CTRLDATA_AUX-	I/OD 3.3 V	PU 100 kΩ 3.3 V	2.2 kΩ to 3.3V pull-up should be implemented on the carrier board.

Signal	Pin #	Description	I/O	PU/PD	Comment
TMDS2_CLK + TMDS2_CLK -	D49 D50	TMDS Clock output differential pair Multiplexed with DDI2_PAIR3+ and DDI2_PAIR3-	O DP		Should be AC-coupled on the carrier board.
TMDS2_DATA0+ TMDS2_DATA0-	D46 D47	TMDS differential pair Multiplexed with DDI2_PAIR2+ and DDI2_PAIR2-	O DP		
TMDS2_DATA1+ TMDS2_DATA1-	D42 D43	TMDS differential pair Multiplexed with DDI2_PAIR1+ and DDI2_PAIR1-	O DP		
TMDS2_DATA2+ TMDS2_DATA2-	D39 D40	TMDS differential pair Multiplexed with DDI2_PAIR0+ and DDI2_PAIR0-	O DP		
HDMI2_HPD	D44	TMDS Hot-plug detect Multiplexed with DDI2_HPD	I DP	PD 100 kΩ	
HDMI2_CTRLCLK	C32	TMDS I^{2}C Control Clock Multiplexed with DDI2_CTRLCLK_AUX+	OD 3.3 V	PD 100 kΩ	2.2 kΩ to 3.3V pull-up should be implemented on the carrier board.
HDM12_CTRLDATA	C33	TMDSI I^{2}C Control Data Multiplexed with DDI2_CTRLDATA_AUX-	I/OD 3.3 V	PU 100 kΩ 3.3 V	2.2 kΩ to 3.3V pull-up should be implemented on the carrier board.
TMDS3_CLK + TMDS3_CLK -	C49 C50	TMDS Clock output differential pair Multiplexed with DDI3_PAIR3+ and DDI3_PAIR3-	O DP		Should be AC-coupled on the carrier board.
TMDS3_DATA0+ TMDS3_DATA0-	C46 C47	TMDS differential pair Multiplexed with DDI3_PAIR2+ and DDI3_PAIR2-	O DP		
TMDS3_DATA1+ TMDS3_DATA1-	C42 C43	TMDS differential pair Multiplexed with DDI3_PAIR1+ and DDI3_PAIR1-	O DP		
TMDS3_DATA2+ TMDS3_DATA2-	C39 C40	TMDS differential pair Multiplexed with DDI3_PAIR0+ and DDI3_PAIR0-	O DP		
HDMI3_HPD	C44	TMDS Hot-plug detect Multiplexed with DDI3_HPD	I DP	PD 100 kΩ	
HDMI3_CTRLCLK	C36	TMDS I^{2}C Control Clock Multiplexed with DDI3_CTRLCLK_AUX+	OD 3.3 V	PD 100 kΩ	2.2 kΩ to 3.3V pull-up should be implemented on the carrier board
HDMI3_CTRLDATA	C37	TMDS I^{2}C Control Data Multiplexed with DDI3_CTRLDATA_AUX-	I/OD 3.3 V	PU 100 kΩ 3.3 V	2.2 kΩ to 3.3V pull-up should be implemented on the carrier board.

Note

The conga-TCV2 does not natively support TMDS. For TMDS support, a DP++ to TMDS converter (e.g. PTN3360D) needs to be implemented..

Table 19 DisplayPort Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
DP1_LANE3+ DP1_LANE3-	D36 D37	Uni-directional main link for the transport of isochronous streams and secondary data Multiplexed with DDI1_PAIR3+ and DDI1_PAIR3-	O DP		Should be AC-coupled on the carrier board.
DP1_LANE2+ DP1_LANE2-	D32 D33	Uni-directional main link for the transport of isochronous streams and secondary data Multiplexed with DDI1_PAIR2+ and DDI1_PAIR2-	O DP		
DP1_LANE1+ DP1_LANE1-	D29 D30	Uni-directional main link for the transport of isochronous streams and secondary data Multiplexed with DDI1_PAIR1+ and DDI1_PAIR1-	O DP		
DP1_LANE0+ DP1_LANE0-	D26 D27	Uni-directional main link for the transport of isochronous streams and secondary data Multiplexed with DDI1_PAIR0+ and DDI1_PAIR0-	O DP		
DP1_HPD	C24	Detection of Hot Plug / Unplug and notification of the link layer. Multiplexed with DDI1_HPD	I 3.3 V	PD 100 kΩ	
DP1_AUX+	D15	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access	I/O DP	PD 100 kΩ	
DP1_AUX-	D16	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access	I/O DP	PU 100 kΩ 3.3 V	
DP2_LANE3+ DP2_LANE3-	D49 D50	Uni-directional main link for the transport of isochronous streams and secondary data Multiplexed with DDI2_PAIR3+ and DDI2_PAIR3-	O DP		Should be AC-coupled on the carrier board.
DP2_LANE2+ DP2_LANE2-	D46 D47	Uni-directional main link for the transport of isochronous streams and secondary data Multiplexed with DDI2_PAIR2+ and DDI2_PAIR2-	O DP		
DP2_LANE1+ DP2_LANE1-	D42 D43	Uni-directional main link for the transport of isochronous streams and secondary data Multiplexed with DDI2_PAIR1+ and DDI2_PAIR1-	O DP		
DP2_LANE0+ DP2_LANE0-	D39 D40	Uni-directional main link for the transport of isochronous streams and secondary data Multiplexed with DDI2_PAIR0+ and DDI1_PAIR0-	O DP		
DP2_HPD	D44	Detection of Hot Plug / Unplug and notification of the link layer. Multiplexed with DDI2_HPD	I 3.3 V	PD 100 kΩ	
DP2_AUX+	C32	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access	I/O DP	PD 100 kΩ	
DP2_AUX-	C33	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access	I/O DP	PU 100 kΩ 3.3 V	
DP3_LANE3+ DP3_LANE3-	C49 C50	Uni-directional main link for the transport of isochronous streams and secondary data Multiplexed with DDI3_PAIR3+ and DDI3_PAIR3-	O DP		Should be AC-coupled on the carrier board.

Signal	Pin #	Description	I/O	PU/PD	Comment
DP3_LANE2+	C46	Uni-directional main link for the transport of isochronous streams and secondary data Multiplexed with DDI3_PAIR2+ and DDI3_PAIR2-.	O DP		Should be AC-coupled on the carrier board.
DP3_LANE2-	C47				
DP3_LANE1+	C42	Uni-directional main link for the transport of isochronous streams and secondary data Multiplexed with DDI3_PAIR1+ and DDI3_PAIR1-	O DP		
DP3_LANE1-	C43				
DP3_LANE0+	C39	Uni-directional main link for the transport of isochronous streams and secondary data Multiplexed with DDI3_PAIR0+ and DDI3_PAIR0-	O DP		
DP3_LANE0-	C40				
DP3_HPD	C44	Detection of Hot Plug / Unplug and notification of the link layer. Multiplexed with DDI3_HPD	I 3.3 V	PD 100 kΩ	
DP3_AUX+	C36	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access	I/O DP	PD 100 kΩ	
DP3_AUX-	C37	Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access	I/O DP	PU 100 kΩ 3.3 V	

Table 20 Embedded DisplayPort Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
eDP_TX3+	A81	eDP differential pairs	AC coupled off module.		
eDP_TX3-	A82				
eDP_TX2+	A71				
eDP_TX2-	A72				
eDP_TX1+	A73				
eDP_TX1-	A74				
eDP_TX0+	A75				
eDP_TX0-	A76				
eDP_VDD_EN	A77	eDP power enable	O 3.3 V		
eDP_BKLT_EN	B79	eDP backlight enable	O 3.3 V		
eDP_BKLT_CTRL	B83	eDP backlight brightness control	O 3.3 V		
eDP_AUX+	A83	eDP AUX+	AC coupled off module		
eDP_AUX-	A84	eDP AUX-	AC coupled off module		
eDP_HPD	A87	Detection of hot plug / unplug and notification of the link layer	I 3.3 V	PD 100 kΩ	

Note

The conga-TCV2 offers eDP interface as an assembly option. LVDS will not be supported if eDP is implemented.

Table 21 CRT Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VGA_RED	B89	Red for monitor; analog DAC output designed to drive a 37.5-Ohm equivalent load	O Analog		Not supported
VGA_GRN	B91	Green for monitor; analog DAC output designed to drive a 37.5-Ohm equivalent load	O Analog		
VGA_BLU	B92	Blue for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load	O Analog		
VGA_HSYNC	B93	Horizontal sync output to VGA monitor	O 3.3 V		
VGA_VSYNC	B94	Vertical sync output to VGA monitor	O 3.3 V		
VGA_I2C_CK	B95	DDC clock line (I²C port dedicated to identify VGA monitor capabilities)	I/O OD 5 V		
VGA_I2C_DAT	B96	DDC data line	I/O OD 5 V		

Note

The conga-TCV2 does not support VGA.

Table 22 LVDS Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LVDS_A0+	A71	LVDS Channel A differential pairs	O LVDS		
LVDS_A0-	A72				
LVDS_A1+	A73				
LVDS_A1-	A74				
LVDS_A2+	A75				
LVDS_A2-	A76				
LVDS_A3+	A78				
LVDS_A3-	A79				
LVDS_A_CK+	A81	LVDS Channel A differential clock	O LVDS		
LVDS_A_CK-	A82				
LVDS_B0+	B71	LVDS Channel B differential pairs	O LVDS		
LVDS_B0-	B72				
LVDS_B1+	B73				
LVDS_B1-	B74				
LVDS_B2+	B75				
LVDS_B2-	B76				
LVDS_B3+	B77				
LVDS_B3-	B78				
LVDS_B_CK+	B81	LVDS Channel B differential clock	O LVDS		
LVDS_B_CK-	B82				
LVDS_VDD_EN	A77	LVDS panel power enable	O 3.3 V	PD 100 kΩ	
LVDS_BKLT_EN	B79	LVDS panel backlight enable	O 3.3 V	PD 100 kΩ	
LVDS_BKLT_CTRL	B83	LVDS panel backlight brightness control	O 3.3 V		
LVDS_I2C_CK	A83	DDC lines used for flat panel detection and control	OD 3.3 V	PU 2.2 kΩ 3.3 V	
LVDS_I2C_DAT	A84	DDC lines used for flat panel detection and control	I/OD 3.3 V	PU 2.2 kΩ 3.3 V	

Table 23 SATA Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SATA0_RX+ SATA0_RX-	A19 A20	Serial ATA channel 0, Receive Input differential pair	I SATA		Supports Serial ATA specification, Revision 3.0. Only two SATA ports can be set to active via BIOS setup menu.
SATA0_TX+ SATA0_TX-	A16 A17	Serial ATA channel 0, Transmit Output differential pair	O SATA		
SATA1_RX+ SATA1_RX-	B19 B20	Serial ATA channel 1, Receive Input differential pair	I SATA		
SATA1_TX+ SATA1_TX-	B16 B17	Serial ATA channel 1, Transmit Output differential pair	O SATA		
SATA2_RX+ SATA2_RX-	A25 A26	Serial ATA channel 2, Receive Input differential pair	I SATA		
SATA2_TX+ SATA2_TX-	A22 A23	Serial ATA channel 2, Transmit Output differential pair	O SATA		
SATA3_RX+ SATA3_RX-	B25 B26	Serial ATA channel 3, Receive Input differential pair	I SATA		
SATA3_TX+ SATA3_TX-	B22 B23	Serial ATA channel 3, Transmit Output differential pair	O SATA		
(S)ATA_ACT#	A28	SATA activity indicator, active low	O 3.3V		Maximum current of 4 mA

Table 24 USB Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
USB0+	A46	Differential USB 2.0 data pairs (backwards compatible to USB 1.1)	I/O USB		
USB0-	A45				
USB1+	B46	Differential USB 2.0 data pairs (backwards compatible to USB 1.1)	I/O USB		Routed from a USB hub on the module.
USB1-	B45				
USB2+	A43	Differential USB 2.0 data pairs (backwards compatible to USB 1.1)	I/O USB		Routed from a USB hub on the module.
USB2-	A42				
USB3+	B43	Differential USB 2.0 data pairs (backwards compatible to USB 1.1)	I/O USB		Routed from a USB hub on the module.
USB3-	B42				
USB4+	A40	Differential USB 2.0 data pairs (backwards compatible to USB 1.1)	I/O USB		
USB4-	A39				
USB5+	B40	Differential USB 2.0 data pairs (backwards compatible to USB 1.1)	I/O USB		
USB5-	B39				
USB6+	A37	Differential USB 2.0 data pairs (backwards compatible to USB 1.1)	I/O USB		
USB6-	A36				
USB7+	B37	Differential USB 2.0 data pairs (backwards compatible to USB 1.1)	I/O USB		
USB7-	B36				

Signal	Pin #	Description	I/O	PU/PD	Comment
USB_SSRX0+	C4	Additional receive signal differential pairs for the Superspeed USB data path	I USB		
USB_SSRX0-	C3		I USB		
USB_SSTX0+	D4	Additional transmit signal differential pairs for the Superspeed USB data path	O USB		
USB_SSTX0-	D3		O USB		
USB_SSRX1+	C7	Additional receive signal differential pairs for the Superspeed USB data path	I USB		Routed from a USB hub on the module.
USB_SSRX1-	C6		I USB		
USB_SSTX1+	D7	Additional transmit signal differential pairs for the Superspeed USB data path	O USB		Routed from a USB hub on the module.
USB_SSTX1-	D6		O USB		
USB_SSRX2+	C10	Additional receive signal differential pairs for the Superspeed USB data path	I USB		Routed from a USB hub on the module.
USB_SSRX2-	C9		I USB		
USB_SSTX2+	D10	Additional transmit signal differential pairs for the Superspeed USB data path	O USB		Routed from a USB hub on the module.
USB_SSTX2-	D9		O USB		
USB_SSRX3+	C13	Additional receive signal differential pairs for the Superspeed USB data path	I USB		Routed from a USB hub on the module.
USB_SSRX3-	C12		I USB		
USB_SSTX3+	D13	Additional transmit signal differential pairs for the Superspeed USB data path	O USB		Routed from a USB hub on the module.
USB_SSTX3-	D12		O USB		
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3 VSB	PU 10 kΩ 3.3 VSB	Do not pull this line high on the carrier board.
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3 VSB	PU 10 kΩ 3.3 VSB	Do not pull this line high on the carrier board.
USB_4_5_OC#	B38	USB over-current sense, USB ports 4 and 5. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3 VSB	PU 10 kΩ 3.3 VSB	Do not pull this line high on the carrier board.
USB_6_7_OC#	A38	USB over-current sense, USB ports 6 and 7. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3 VSB	PU 10 kΩ 3.3 VSB	Do not pull this line high on the carrier board.

Table 25 Gigabit Ethernet Signal Descriptions

<table>
<tr><th>Gigabit Ethernet</th><th>Pin #</th><th>Description</th><th>I/O</th><th>PU/PD</th><th>Comment</th></tr>
<tr><td>GBE0_MDI0+
GBE0_MDI0-
GBE0_MDI1+
GBE0_MDI1-
GBE0_MDI2+
GBE0_MDI2-
GBE0_MDI3+
GBE0_MDI3-</td><td>A13
A12
A10
A9
A7
A6
A3
A2</td><td>Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100, and 10 Mb/s modes. Some pairs are unused in some modes according to the following:
<table>
<tr><th></th><th>1000</th><th>100</th><th>10</th></tr>
<tr><td>MDI[0]+/-</td><td>B1_DA+/-</td><td>TX+/-</td><td>TX+/-</td></tr>
<tr><td>MDI[1]+/-</td><td>B1_DB+/-</td><td>RX+/-</td><td>RX+/-</td></tr>
<tr><td>MDI[2]+/-</td><td>B1_DC+/-</td><td></td><td></td></tr>
<tr><td>MDI[3]+/-</td><td>B1_DD+/-</td><td></td><td></td></tr>
</table></td><td>I/O Analog</td><td></td><td>Twisted pair signals for external transformer.</td></tr>
<tr><td>GBE0_ACT#</td><td>B2</td><td>Gigabit Ethernet Controller 0 activity indicator, active low</td><td>O 3.3 VSB</td><td></td><td></td></tr>
<tr><td>GBE0_LINK#</td><td>A8</td><td>Gigabit Ethernet Controller 0 link indicator, active low</td><td>O 3.3 VSB</td><td></td><td></td></tr>
<tr><td>GBE0_LINK100#</td><td>A4</td><td>Gigabit Ethernet Controller 0 100 Mb/s link indicator, active low</td><td>O 3.3 VSB</td><td></td><td></td></tr>
<tr><td>GBE0_LINK1000#</td><td>A5</td><td>Gigabit Ethernet Controller 0 1000 Mb/s link indicator, active low</td><td>O 3.3 VSB</td><td></td><td></td></tr>
<tr><td>GBE0_CTREF</td><td>A14</td><td>Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module PHY and may be as low as 0 V and as high as 3.3 V. The reference voltage output shall be current limited on the module. In the case in which the reference is shorted to ground, the current shall be limited to 250 mA or less.</td><td></td><td></td><td>Not connected</td></tr>
</table>

Note

1. *The MAC address of the Intel i225 Ethernet controller is preprogrammed by default. The MAC address cannot be reprogrammed. If you require custom MAC address, contact your local sales representative.*

2. *The GBE0_LINK# output is not active during a 10 Mb connection. It is only active during a 100 Mb, 1 Gb or 2.5 Gb connection. This is a limitation of Ethernet controller since it only has 3 LED outputs—ACT#, LINK100# and LINK1000#.*

3. *The GBE0_LINK# signal is a logic AND of the GBE0_LINK100# and GBE0_LINK1000# signals on the conga-TCV2 module. The LINK1000# output is active during 1 Gb and 2.5 Gb connection. The ACT# output is active during LINK#, LINK100# and LINK1000# (all speed). The LEDs blink when an activity is detected.*

Table 26 High Definition Audio Link Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
HDA_RST#	A30	Reset output to codec, active low	O 3.3 VSB		
HDA_SYNC	A29	Sample-synchronization signal to the codec(s)	O 3.3 VSB		
HDA_BITCLK	A32	Serial data clock generated by the external codec(s)	O 3.3 VSB		
HDA_SDOUT	A33	Serial TDM data output to the codec	O 3.3 VSB		
HDA_SDIN[2:0]	B28-B30	Serial TDM data inputs from up to three codecs	I 3.3 VSB	PD 47 kΩ	

Table 27 LPC Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
LPC_AD[0:3]	B4-B7	LPC Mode: LPC multiplexed address, command and data bus	I/O 3.3 V	PU 50 kΩ 3.3 V	
LPC_FRAME#	B3	LPC Mode: LPC Frame indicates the start of a LPC cycle	O 3.3 V		
LPC_CLK	B10	LPC Mode: LPC clock output, 33MHz	O 3.3 V		
LPC_DRQ0#	B8	LPC Mode: LPC serial DMA request	I 3.3 V	PU 10 kΩ 3.3 V	
LPC_DRQ1#	B9	LPC Mode: LPC serial DMA request	I 3.3 V		Not connected
LPC_SERIRQ	A50	LPC Mode: LPC serial interrupt	I/O 3.3 V	PU 50 kΩ 3.3 V	
SUS_STAT#	B18	LPC Mode: Indicates imminent suspend operation. It is used to notify LPC devices that a low power state will be entered soon. LPC devices may need to preserve memory or isolate outputs during the low power state.	O 3.3 V		

Note

The conga-TCV2 does not support ESPI mode.

Table 28 SPI BIOS Flash Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SPI_CS#	B97	Chip select for Carrier Board SPI BIOS Flash	O 3.3 VSB		
SPI_MISO	A92	Data in to module from carrier board SPI BIOS flash	I 3.3 VSB		
SPI_MOSI	A95	Data out from module to carrier board SPI BIOS flash	O 3.3 VSB		
SPI_CLK	A94	Clock from module to carrier board SPI BIOS flash	O 3.3 VSB		
SPI_POWER	A91	Power source for carrier board SPI BIOS flash. SPI_POWER shall be used to power SPI BIOS flash on the carrier only	P 3.3 VSB		
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device	I 3.3 VSB	PU 10 kΩ 3.3 VSB	Carrier shall pull to GND or left as no-connect.
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device	I 3.3 VSB	PU 10 kΩ 3.3 VSB	Carrier shall pull to GND or left as no-connect.

Table 29 Miscellaneous Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
I2C_CK	B33	General purpose I²C port clock output/input	I/OD 3.3 V	PU 2.2 kΩ 3.3 VSB	
I2C_DAT	B34	General purpose I²C port data I/O line	I/OD 3.3 V	PU 2.2 kΩ 3.3 VSB	
SPKR	B32	Output for audio enunciator, the "speaker" in PC-AT systems	O 3.3 V		
WDT	B27	Output indicating that a watchdog time-out event has occurred	O 3.3 V		
FAN_PWMOUT [1]	B101	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	O OD 3.3 V		Signal is driven to logic 1 or high impedance only. External 4.7 kΩ PD is required on the carrier board
FAN_TACHIN [1]	B102	Fan tachometer input	I OD	PU 47 kΩ 3.3 V	Requires a fan with two-pulse output.
TPM_PP	A96	Physical Presence pin of Trusted Platform Module (TPM). Active high. TPM chip has an internal pull-down. This signal is used to indicate Physical Presence to the TPM.	I 3.3 V	PD 10 kΩ	A TPM 2.0 chip is assembled on the module by default.

Note

[1] *Pins are protected on the module by a series schottky diode.*

Table 30 General Purpose I/O Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
GPO0	A93	General purpose output pins	O 3.3 V		
GPO1	B54	General purpose output pins	O 3.3 V		
GPO2	B57	General purpose output pins	O 3.3 V		
GPO3	B63	General purpose output pins	O 3.3 V		
GPI0	A54	General purpose input pins. Pulled high internally on the module	I 3.3 V	PU 80 kΩ 3.3 V	
GPI1	A63	General purpose input pins. Pulled high internally on the module	I 3.3 V	PU 80 kΩ 3.3 V	
GPI2	A67	General purpose input pins. Pulled high internally on the module	I 3.3 V	PU 80 kΩ 3.3 V	
GPI3	A85	General purpose input pins. Pulled high internally on the module	I 3.3 V	PU 80 kΩ 3.3 V	

Table 31 Power and System Management Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
PWRBTN#	B12	Power button to bring system out of S5 (soft off), active on falling edge Note: For proper detection, assert a pulse width of at least 16 ms	I 3.3 VSB	PU 10 kΩ 3.3 VSB	
SYS_RESET#	B49	Reset button input. Active low input. Edge triggered System will not be held in hardware reset while this input is kept low Note: For proper detection, assert a pulse width of at least 16 ms	I 3.3 VSB	PU 10 kΩ 3.3 VSB	

Signal	Pin #	Description	I/O	PU/PD	Comment
CB_RESET#	B50	Reset output from module to Carrier Board Active low, issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.	O 3.3 V		
PWR_OK	B24	Power OK from main power supply. A high value indicates that the power is good	I 3.3 V	PU 10 kΩ 3.3 V	Set by resistor divider to accept 3.3V
SUS_STAT#	B18	Indicates imminent suspend operation; used to notify LPC devices	O 3.3 VSB		
SUS_S3#	A15	Indicates system is in Suspend to RAM state. Active-low output. An inverted copy of SUS_S3# on the carrier board (also known as "PS_ON") may be used to enable the non-standby power on a typical ATX power supply.	O 3.3 VSB		
SUS_S4#	A18	Indicates system is in Suspend to Disk state. Active low output	O 3.3 VSB		Not supported (connected to SUS_S5# on module)
SUS_S5#	A24	Indicates system is in Soft Off state	O 3.3 VSB		
WAKE0#	B66	PCI Express wake up signal	I 3.3 VSB	PU 10 kΩ 3.3 VSB	
WAKE1#	B67	General purpose wake up signal May be used to implement wake-up on PS/2 keyboard or mouse activity	I 3.3 VSB	PU 10 kΩ 3.3 VSB	
BATLOW#	A27	Battery low input This signal may be driven low by external circuitry to signal that the system battery is low, or may be used to signal some other external power-management event.	I 3.3 VSB	PU 10 kΩ 3.3 VSB	
LID# [1]	A103	Lid button used by the ACPI operating system for a LID switch Note: For proper detection, assert a pulse width of at least 16 ms.	I 3.3 V	PU 47 kΩ 3.3 V	
SLEEP# [1]	B103	Sleep button used by the ACPI operating system to bring the system to sleep state or to wake it up again Note: For proper detection, assert a pulse width of at least 16 ms.	I 3.3 V	PU 47 kΩ 3.3 V	

Note

[1] *Pins are protected on the module by a series schottky diode.*

Table 32 Rapid Shutdown Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
RAPID_SHUTDOWN	C67	Trigger for Rapid Shutdown. Must be driven to 5V though a <=50 ohm source impedance for ≥ 20 µs	I 3.3 V		Not connected

Note

The conga-TCV2 does not support Rapid Shutdown.

Table 33 Thermal Protection Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
THRM#	B35	Input from off-module temp sensor indicating an over-temp situation	I 3.3 V	PU 10 kΩ 3.3 V	
THRMTRIP#	A35	Active low output indicating that the CPU has entered thermal shutdown	O 3.3 V	PU 1 kΩ 3.3 V	

Table 34 SMBus Signal Description

Signal	Pin #	Description	I/O	PU/PD	Comment
SMB_CK	B13	System Management Bus bidirectional clock line	I/O 3.3 VSB	PU 2.2 kΩ 3.3 VSB	
SMB_DAT#	B14	System Management Bus bidirectional data line	I/O OD 3.3 VSB	PU 2.2 kΩ 3.3 VSB	
SMB_ALERT#	B15	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.	I 3.3 VSB	PU 10 kΩ 3.3 VSB	

Table 35 General Purpose Serial Interface Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
SER0_TX [1,2]	A98	General purpose serial port transmitter	O 3.3 V		
SER1_TX [1,2]	A101	General purpose serial port transmitter	O 3.3 V		
SER0_RX [1]	A99	General purpose serial port receiver	I 3.3 V	PU 47 kΩ 3.3 V	
SER1_RX [1]	A102	General purpose serial port receiver	I 3.3 V	PU 47 kΩ 3.3 V	

Note

[1] *Pins are protected on the module by a series schottky diode.*

[2] *Signal is driven to logic 1 or high impedance only. An external 4.7 K pull-down resistor is required on the carrier board for proper logic level.*

Table 36 Module Type Definition Signal Description

<table>
<tr><th>Signal</th><th>Pin #</th><th colspan="4">Description</th><th>I/O</th><th>Comment</th></tr>
<tr><td rowspan="4">TYPE0#
TYPE1#
TYPE2#</td><td rowspan="4">C54
C57
D57</td><td colspan="4">The TYPE pins indicate to the carrier board the pinout type that is implemented on the module.

The pins are tied on the module to either ground (GND) or are no-connects (NC). For pinout Type 1, these pins are don’t care (X).</td><td rowspan="4">PDS</td><td rowspan="4">TYPE[0:2]# signals are available on all modules following the Type 2-6 Pinout standard.

The conga-TCV2 is based on the COM Express® Type 6 pinout therefore the pins 0 and 1 are not connected and pin 2 is connected to GND.</td></tr>
<tr><td>TYPE2#</td><td>TYPE1#</td><td>TYPE0#</td><td></td></tr>
<tr><td>X
NC
NC
NC
NC
GND</td><td>X
NC
NC
GND
GND
NC</td><td>X
NC
GND
NC
GND
NC</td><td>Pinout Type 1
Pinout Type 2
Pinout Type 3 (no IDE)
Pinout Type 4 (no PCI)
Pinout Type 5 (no IDE, no PCI)
Pinout Type 6 (no IDE, no PCI)</td></tr>
<tr><td colspan="4">The carrier board should implement combinatorial logic that monitors the module ‘TYPE’ pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible module pin-out type is detected.

The carrier board logic may also implement a fault indicator such as an LED.</td></tr>
<tr><td rowspan="4">TYPE10#</td><td rowspan="4">A97</td><td colspan="4">Dual use pin.
Indicates to the carrier board that a Type 10 module is installed.
Indicates to the carrier that a Rev. 1.0/2.0 module is installed.</td><td rowspan="4">PDS</td><td rowspan="4">Not connected to indicate “Pinout R2.0”.</td></tr>
<tr><td colspan="4">TYPE10#</td></tr>
<tr><td colspan="2">NC
PD
12V</td><td colspan="2">Pinout R2.0
Pinout Type 10 pull down to ground with 4.7k resistor
Pinout R1.0</td></tr>
<tr><td colspan="4">This pin is reclaimed from VCC_12V pool. In R1.0 modules this pin will connect to other VCC_12V pins.

In R2.0 this pin is defined as a no-connect for Types 1-6. A carrier can detect a R1.0 module by the presence of 12 V on this pin. R2.0 module Types 1-6 will no-connect this pin. Type 10 modules shall pull this pin to ground through a 4.7 kΩ resistor.</td></tr>
</table>

Table 37 Power and GND Signal Descriptions

Signal	Pin #	Description	I/O	PU/PD	Comment
VCC_12V	A104-A109 B104-B109 C104-C109 D104-D109	Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.	P		
VCC_5V_SBY	B84-B87	Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.	P		
VCC_RTC	A47	Real-time clock circuit-power input. Nominally +3.0V.	P		
GND	A1, A11, A21, A31, A41, A51, A57, A60, A66, A70, A80, A90, A100, A110, B1, B11, B21, B31, B41, B51, B60, B70, B80, B90, B100, B110 C1, C2, C5, C8, C11, C14, C21, C31, C41, C51, C60, C70,C73, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110, D1, D2, D5, D8, D11, D14, D21, D31, D41, D51, D60, D67, D70, D73, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110	Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane.	P		

8.2 Bootstrap Signals

Table 38 Bootstrap Signal Descriptions

Signal	Pin #	Description of Bootstrap Signal	I/O	PU/PD	Comment
SPI_CLK	A94	Clock from moduel to carrier board SPI BIOS flash	O 3.3 VSB		Do not use any PU/PD on the carrier board

Caution

1. *The signals listed in the table above are used as chipset configuration straps during system reset. In this condition (during reset), they are inputs that are pulled to the correct state by either COM Express® internally implemented resistors or chipset internally implemented resistors that are located on the module.*

2. *No external DC loads or external pull-up or pull-down resistors should change the configuration of the signals listed in the above table. External resistors may override the internal strap states and cause the COM Express® module to malfunction and/or cause irreparable damage to the module.*

9 System Resources

9.1 I/O Address Assignment

The I/O address assignment of the conga-T module is functionally identical with a standard PC/AT.

Note

The BIOS assigns PCI and PCI Express I/O resources from FFF0h downwards. Non PnP/PCI/PCI Express compliant devices must not consume I/O resources in that area.

9.1.1 LPC Bus

On the conga-TC370, the PCI Express Bus acts as the subtractive decoding agent. All I/O cycles that are not positively decoded are forwarded to the PCI Bus not the LPC Bus. Only specified I/O ranges are forwarded to the LPC Bus. In the congatec Embedded BIOS the following I/O address ranges are sent to the LPC Bus:

2Eh – 2Fh
4Eh – 4Fh
60h, 64h
A00h – A1Fh
E00h - EFFh (always used internally)

Parts of these ranges are not available if a Super I/O is used on the carrier board. If a Super I/O is not implemented on the carrier board then these ranges are available for customer use. If you require additional LPC Bus resources other than those mentioned above, or more information about this subject, contact congatec technical support for assistance.

9.2 PCI Configuration Space Map

Table 39 PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00h	00h	00h	Root Complex
00h	00h	02h	IOMMU
00h	01h	00h	PCIe® Dummy Host Bridge
00h (Note1)	01h	01h	PCI Express PEG Port 0
00h (Note1)	01h	02h	PCI Express PEG Port 1
00h	01h	03h	PCI Express port for Ethernet
00h	02h	00h	PCIe® Dummy Host Bridge
00h (Note1)	02h	01h	PCI Express Port 0
00h (Note1)	02h	02h	PCI Express Port 1
00h (Note1)	02h	03h	PCI Express Port 2
00h (Note1)	02h	04h	PCI Express Port 3 or PCI Express Port 7 (Note2)
00h (Note1)	02h	05h	PCI Express Port 4
00h (Note1)	02h	06h	PCI Express Port 5
00h (Note1)	02h	07h	PCI Express Port 6
00h	08h	00h	PCIe® Dummy Host Bridge
00h	08h	01h	Internal PCIe® GPP Bridge 0 to Bus B
00h	08h	02h	Internal PCIe® GPP Bridge 1 to Bus C
00h	14h	00h	AMD SMBus Controller
00h	14h	03h	LPC Bridge
00h	18h	00h	Data Fabric
00h	18h	01h	Data Fabric
00h	18h	02h	Data Fabric
00h	18h	03h	Data Fabric
00h	18h	04h	Data Fabric
00h	18h	05h	Data Fabric
00h	18h	06h	Data Fabric
00h	18h	07h	Data Fabric
01h (Note3)	00h	00h	PCIe device inserted in PCI Express PEG Port 0
02h (Note3)	00h	00h	PCIe device inserted in PCI Express PEG Port 1

03h (Note3)	00h	00h	Intel Ethernet controller I225 in PCI Express port for Ethernet
04h (Note3)	00h	00h	PCIe device inserted in PCI Express Port 0
05h (Note3)	00h	00h	PCIe device inserted in PCI Express Port 1
06h (Note3)			PCIe device inserted in PCI Express Port 2
07h (Note3)	00h	00h	PCIe device inserted in PCI Express Port 3 or PCI Express Port 7 (Note2)
08h (Note3)	00h	00h	PCIe device inserted in PCI Express Port 4
09h (Note3)	00h	00h	PCIe device inserted in PCI Express Port 5
0Ah (Note3)	00h	00h	PCIe device inserted in PCI Express Port 6
0Bh (Note 4)	00h	00h	Integrated Graphics Device
0Bh (Note 4)	00h	01h	Display HD Audio Controller
0Bh (Note 4)	00h	02h	Cryptographic Coprocessor (PSP/CCP)
0Bh (Note 4)	00h	03h	USB3.1 Controller (USB0)
0Bh (Note 4)	00h	04h	USB3.1 Controller (USB1)
0Bh (Note 4)	00h	05h	Audio Processor (ACP)
0Bh (Note 4)	00h	06h	Audio Processor – HD Audio Controller
0Bh (Note 4)	00h	07h	Sensor Fusion Hub (MP2)
0Ch (Note 4)	00h	00h	SATA AHCI mode with MS driver support

Note

1. *The PCI Express ports are visible only if a device is attached to the PCI Express slot on the carrier board.*

2. *PCI Express port 3 is Bus 0: Dev 2: Fun 4 in most PCIe configurations. However, if the PCI Express port 0-7 is configured to 1 x4 or 4 x1 link, the PCI Express Port 7 becomes Bus 0: Dev 2: Fun 4.*

3. *The table represents a case when a single functional PCI/PCIe device is connected to all possible slots on the carrier board. The given bus numbers will change based on actual hardware configuration.*

4. *Internal and integrated controller. The bus numbers B and C are flexible and behind the PCIe Device Bus number.*

5. *Internal PCI devices that are not connected to the conga-TCV2 are not listed.*

9.3 I^{2}C

Onboard resources are not connected to the I^{2}C bus. Address 16h is reserved for congatec Battery Management solutions.

9.4 SMBus

The SMBus signals are also connected to the Intel® chipset. The SMBus is not intended to be used by off-board non-system management devices. For more information about this subject, contact congatec technical support.

10 BIOS Setup Description

The BIOS setup description of the conga-TCV2 can be viewed without having access to the module. However, access to the restricted area of the congatec website is required in order to download the necessary tool (CgMlfViewer) and Menu Layout File (MLF).

The MLF contains the BIOS setup description of a particular BIOS revision. The MLF can be viewed with the CgMlfViewer tool. This tool offers a search function to quickly check for supported BIOS features. It also shows where each feature can be found in the BIOS setup menu.

For more information, read the application note "AN42 - BIOS Setup Description" available at www.congatec.com.

Note

If you do not have access to the restricted area of the congatec website, contact your local congatec sales representative.

10.1 Navigating the BIOS Setup Menu

The BIOS setup menu shows the features and options supported in the congatec BIOS. To access and navigate the BIOS setup menu, press the <DEL> or <F2> key during POST.

The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

10.2 BIOS Versions

The BIOS displays the BIOS project name and the revision code during POST, and on the main setup screen. The initial production BIOS for conga-TCV2 is identified as TCV2R1xx, where:

- R is the identifier for a BIOS ROM file,
- 1 is the so called feature number and
- xx is the major and minor revision number.

The conga-TCV2 binary size is 16 MB.

10.3 Updating the BIOS

BIOS updates are recommended to correct platform issues or enhance the feature set of the module. The conga-TCV2 features a congatec/AMI AptioEFI firmware on an onboard flash ROM chip. You can update the firmware with the congatec System Utility. The utility has five versions— UEFI shell, DOS based command line[1], Win32 command line, Win32 GUI, and Linux version.

For more information about "Updating the BIOS" refer to the user's guide for the congatec System Utility "CGUTLm1x.pdf" on the congatec website at www.congatec.com.

Note

[1] *Deprecated*

Caution

The DOS command line tool is not officially supported by congatec and therefore not recommended for critical tasks such as firmware updates. We recommend to use only the UEFI shell for critical updates.

10.4 Supported Flash Devices

The conga-TCV2 supports the following flash device:

- W25Q128JVSIQ (16 MB)

The flash device listed above can be used on the carrier board to support external BIOS. For more information about external BIOS support, refer to the Application Note AN7_External_BIOS_Update.pdf on the congatec website at http://www.congatec.com.